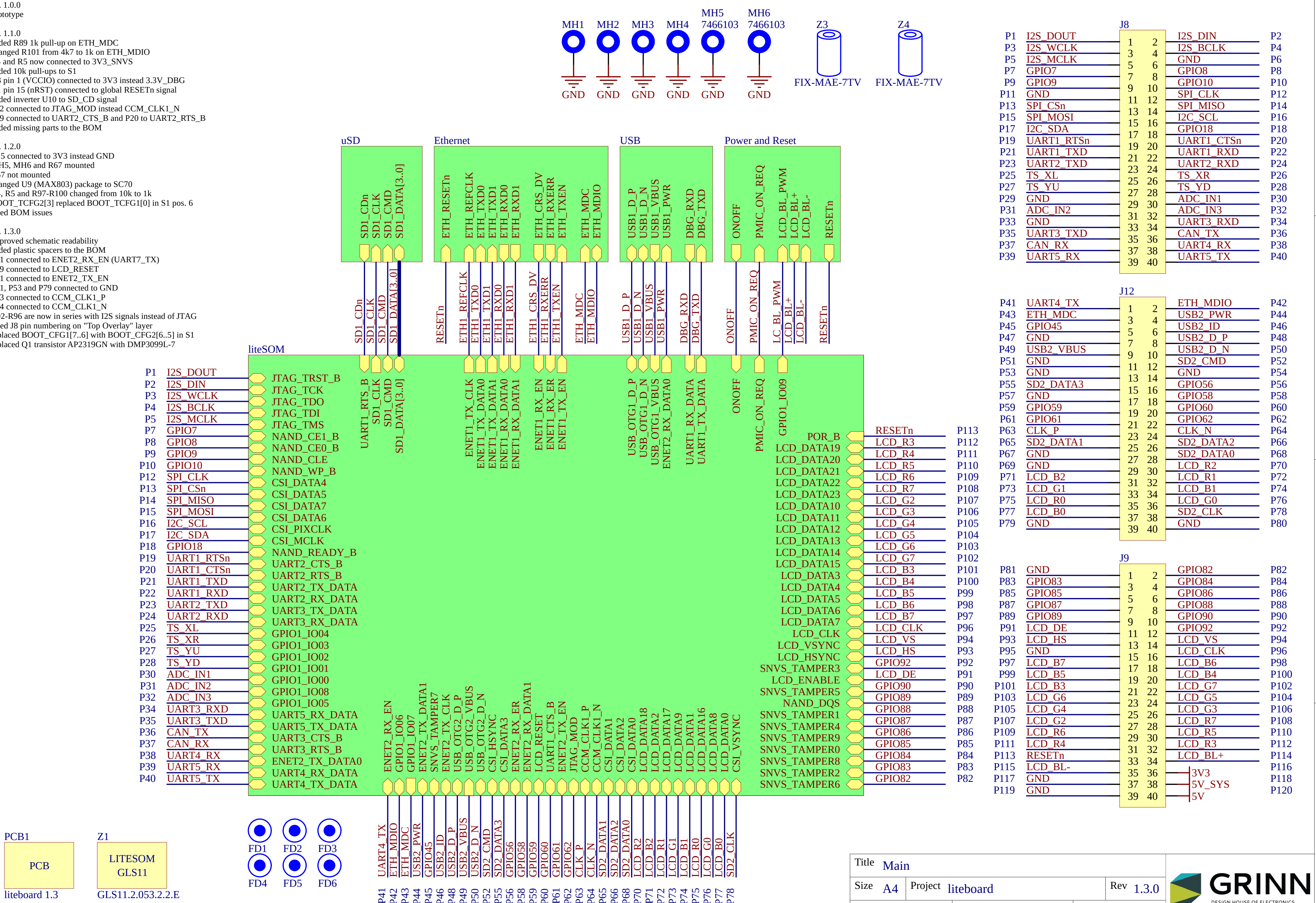
Rev. 1.0.0
- prototype

Rev. 1.1.0
- added R89 1k pull-up on ETH_MDC
- changed R101 from 4k7 to 1k on ETH_MDIO
- R4 and R5 now connected to 3V3_SNVS
- added 10k pull-ups to S1
- U3 pin 1 (VCCIO) connected to 3V3 instead 3.3V_DBG
- U1 pin 15 (nRST) connected to global RESETn signal
- added inverter U10 to SD_CD signal
- P62 connected to JTAG_MOD instead CCM_CLK1_N
- P19 connected to UART2_CTS_B and P20 to UART2_RTS_B
- added missing parts to the BOM

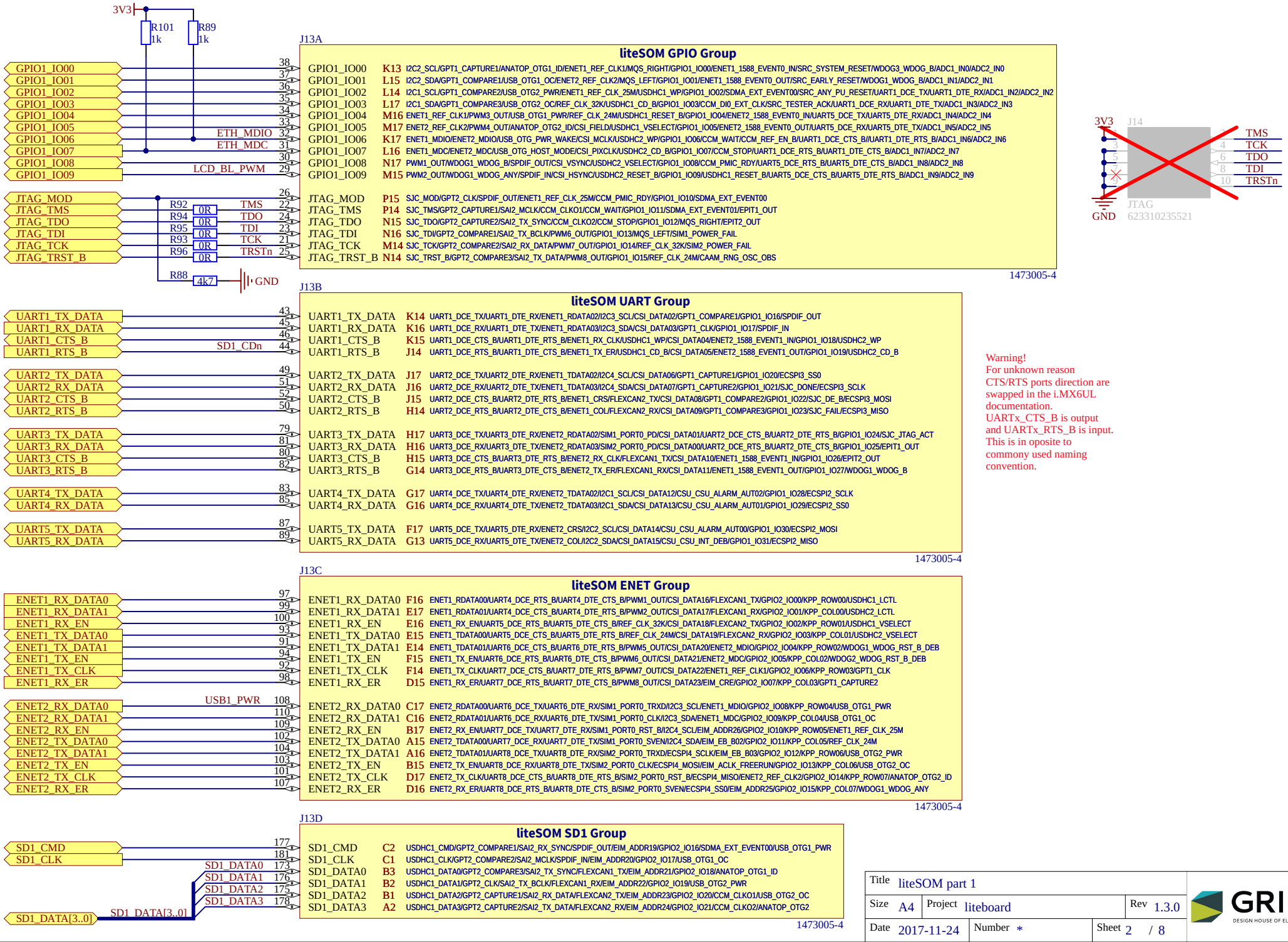
Rev. 1.2.0
- R15 connected to 3V3 instead GND
- MH5, MH6 and R67 mounted
- R67 not mounted
- changed U9 (MAX803) package to SC70
- R4, R5 and R97-R100 changed from 10k to 1k
- BOOT_TCFG2[3] replaced BOOT_TCFG1[0] in S1 pos. 6
- fixed BOM issues

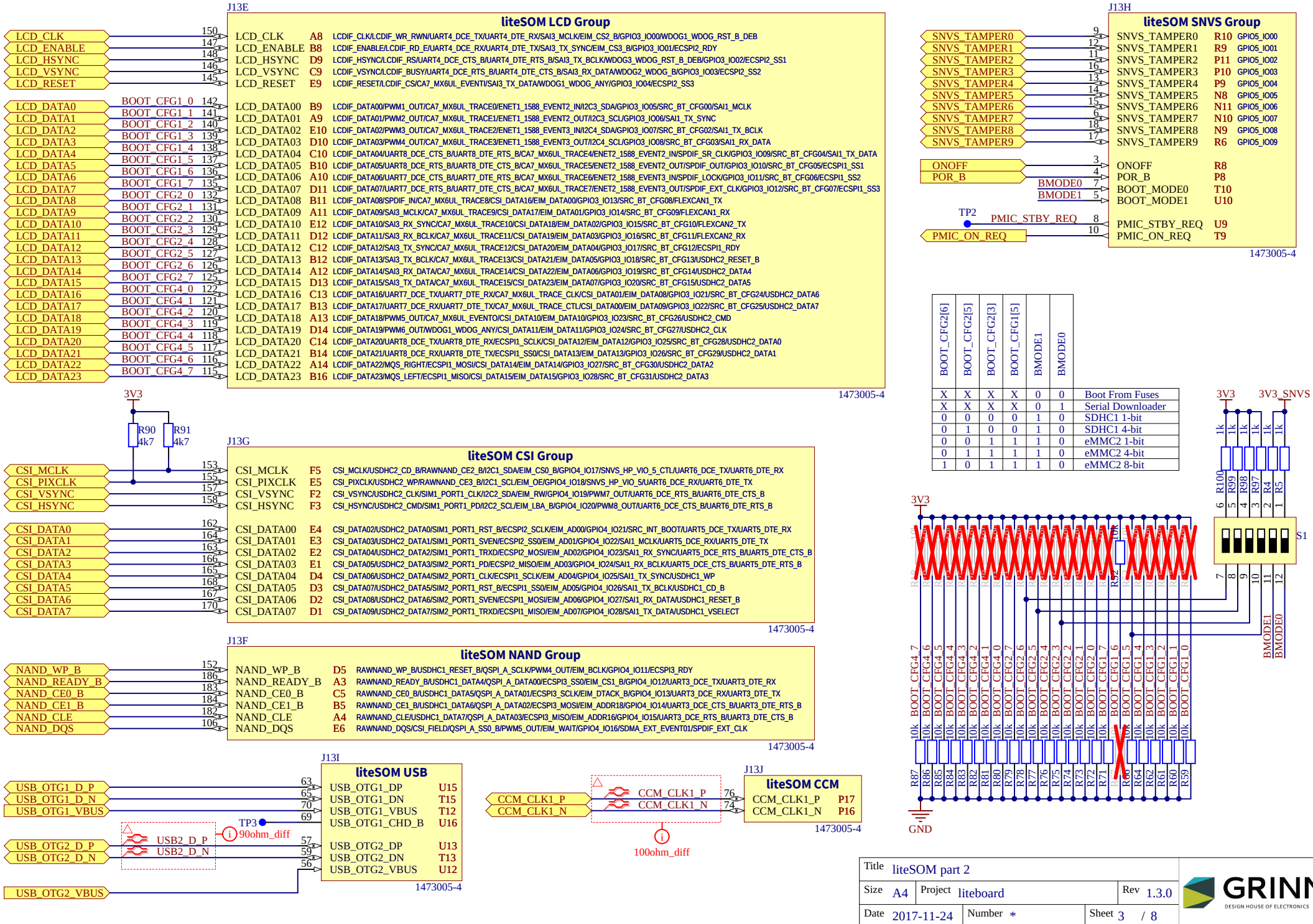
Rev. 1.3.0
- improved schematic readability
- added plastic spacers to the BOM
- P41 connected to ENET2_RX_EN (UART7_TX)
- P59 connected to LCD_RESET
- P61 connected to ENET2_TX_EN
- P51, P53 and P79 connected to GND
- P63 connected to CCM_CLK1_P
- P64 connected to CCM_CLK1_N
- R92-R96 are now in series with I2S signals instead of JTAG
- fixed J8 pin numbering on "Top Overlay" layer
- replaced BOOT_CFG1[7..6] with BOOT_CFG2[6..5] in S1
- replaced Q1 transistor AP2319GN with DMP3099L-7

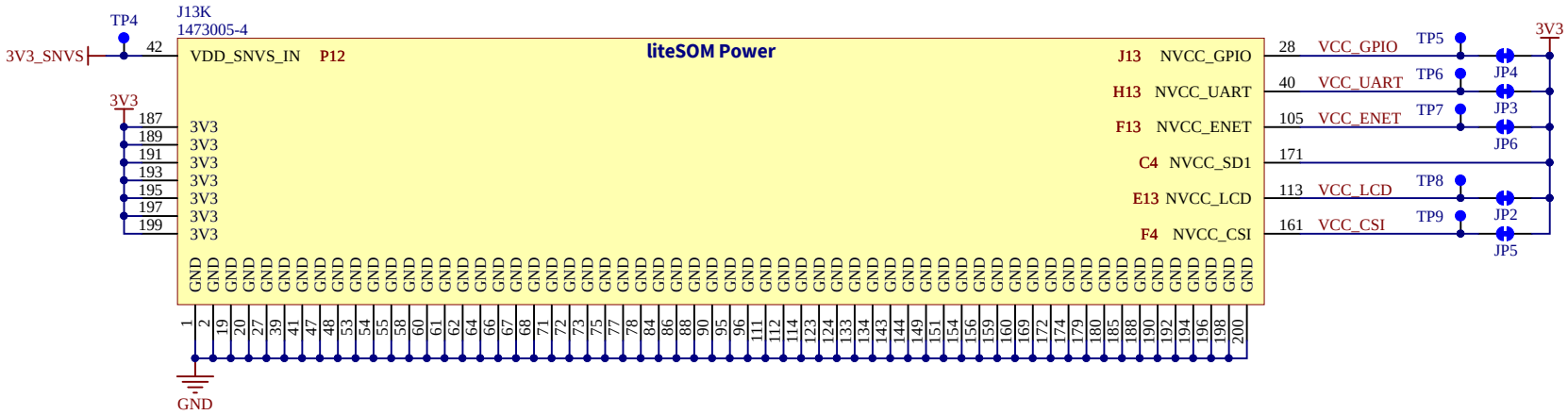


Title	Main				
Size	A4	Project	liteboard	Rev	1.3.0
Date	2017-11-24	Number		Sheet	1 / 8

GRINN
DESIGN HOUSE OF ELECTRONICS

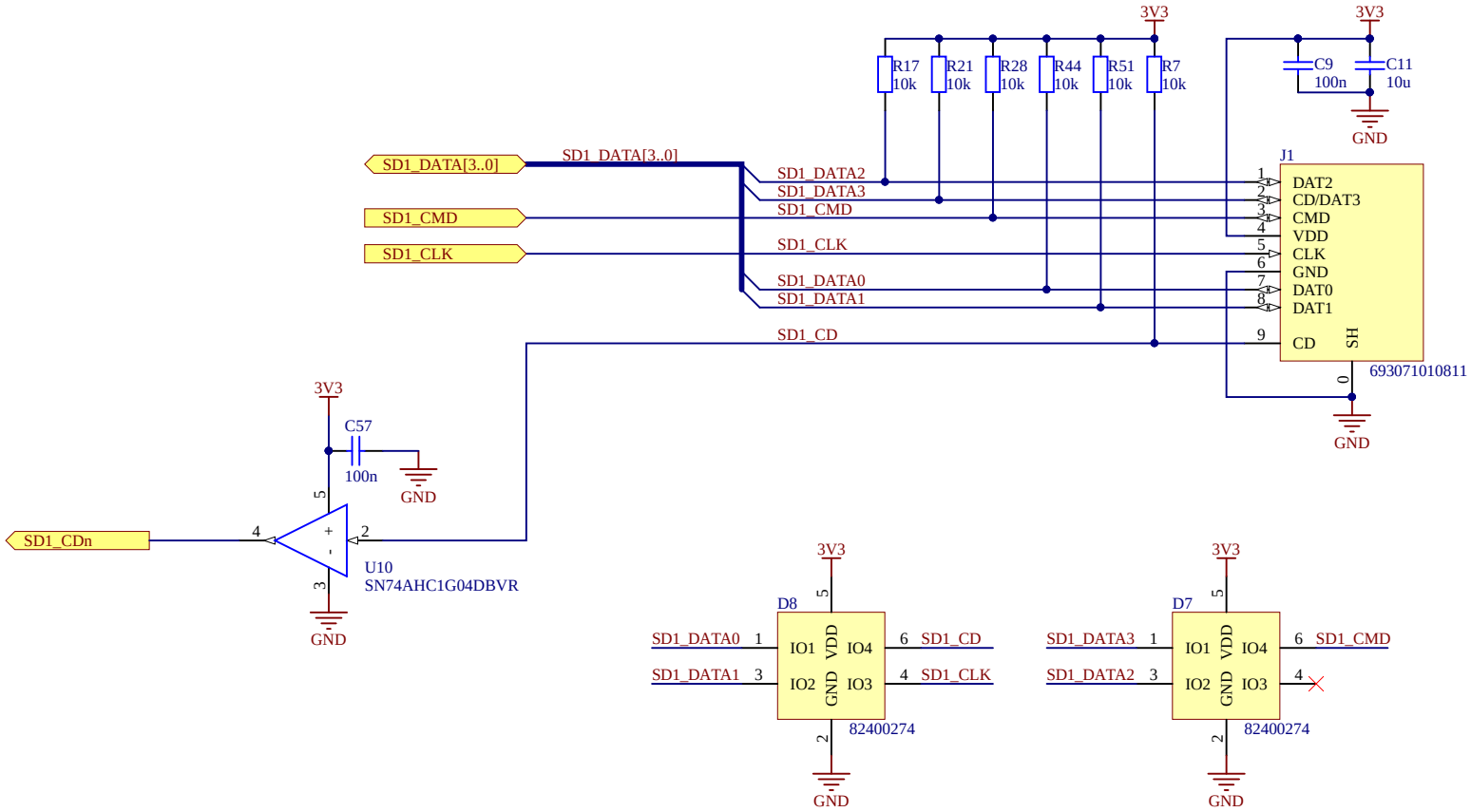

3V3
R101 1k
R89 1k
J13A
liteSOM GPIO Group
GPIO1_IO00 K13 I2C2_SCL/GPT1_CAPTURE1/ANATOP_OTG1_ID/ENET1_REF_CLK1/MQS_RIGHT/GPIO1_IO00/ENET1_1588_EVENT0_IN/SRC_SYSTEM_RESET/WDOG3_WDOG_B/ADC1_IN0/ADC2_IN0
GPIO1_IO01 L15 I2C2_SDA/GPT1_COMPARE1/USB_OTG1_OC/ENET2_REF_CLK2/MQS_LEFT/GPIO1_IO01/ENET1_1588_EVENT0_OUT/SRC_EARLY_RESET/WDOG1_WDOG_B/ADC1_IN1/ADC2_IN1
GPIO1_IO02 L14 I2C1_SCL/GPT1_COMPARE2/USB_OTG2_PWR/ENET1_REF_CLK_25M/USDHC1_WP/GPIO1_IO02/SDMA_EXT_EVENT00/SRC_ANY_PU_RESET/UART1_DCE_TX/UART1_DTE_RX/ADC1_IN2/ADC2_IN2
GPIO1_IO03 L17 I2C1_SDA/GPT1_COMPARE3/USB_OTG2_OC/REF_CLK_32K/USDHC1_CD_B/GPIO1_IO03/CCM_DI0_EXT_CLK/SRC_TESTER_ACK/UART1_DCE_RX/UART1_DTE_TX/ADC1_IN3/ADC2_IN3
GPIO1_IO04 M16 ENET1_REF_CLK1/PWM3_OUT/USB_OTG1_PWR/REF_CLK_24M/USDHC1_RESET_B/GPIO1_IO04/ENET2_1588_EVENT0_IN/UART5_DCE_TX/UART5_DTE_RX/ADC1_IN4/ADC2_IN4
GPIO1_IO05 M17 ENET2_REF_CLK2/PWM4_OUT/ANATOP_OTG2_ID/CSI_FIELD/USDHC1_VSELECT/GPIO1_IO05/ENET2_1588_EVENT0_OUT/UART5_DCE_RX/UART5_DTE_TX/ADC1_IN5/ADC2_IN5
GPIO1_IO06 K17 ENET1_MDIO/ENET2_MDIO/USB_OTG_PWR_WAKE/CSI_MCLK/USDHC2_WP/GPIO1_IO06/CCM_WAIT/CCM_REF_EN_B/UART1_DCE_CTS_B/UART1_DTE_RTS_B/ADC1_IN6/ADC2_IN6
GPIO1_IO07 L16 ENET1_MDC/ENET2_MDC/USB_OTG_HOST_MODE/CSI_PIXCLK/USDHC2_CD_B/GPIO1_IO07/CCM_STOP/UART1_DCE_RTS_B/UART1_DTE_CTS_B/ADC1_IN7/ADC2_IN7
GPIO1_IO08 N17 PWM1_OUT/WDOG1_WDOG_B/SPDIF_OUT/CSI_VSYNC/USDHC2_VSELECT/GPIO1_IO08/CCM_PMIC_RDY/UART5_DCE_RTS_B/UART5_DTE_CTS_B/ADC1_IN8/ADC2_IN8
GPIO1_IO09 M15 PWM2_OUT/WDOG1_WDOG_ANY/SPDIF_IN/CSI_HSYNC/USDHC2_RESET_B/GPIO1_IO09/USDHC1_RESET_B/UART5_DCE_CTS_B/UART5_DTE_RTS_B/ADC1_IN9/ADC2_IN9
JTAG_MOD P15 SJC_MOD/GPT2_CLK/SPDIF_OUT/ENET1_REF_CLK_25M/CCM_PMIC_RDY/GPIO1_IO10/SDMA_EXT_EVENT00
JTAG_TMS P14 SJC_TMS/GPT2_CAPTURE1/SAI2_MCLK/CCM_CLKO1/CCM_WAIT/GPIO1_IO11/SDMA_EXT_EVENT01/EPIT1_OUT
JTAG_TDO N15 SJC_TDO/GPT2_CAPTURE2/SAI2_TX_SYNC/CCM_CLKO2/CCM_STOP/GPIO1_IO12/MQS_RIGHT/EPIT2_OUT
JTAG_TDI N16 SJC_TDI/GPT2_COMPARE1/SAI2_TX_BCLK/PWM6_OUT/GPIO1_IO13/MQS_LEFT/SIM1_POWER_FAIL
JTAG_TCK M14 SJC_TCK/GPT2_COMPARE2/SAI2_RX_DATA/PWM7_OUT/GPIO1_IO14/REF_CLK_32K/SIM2_POWER_FAIL
JTAG_TRST_B N14 SJC_TRST_B/GPT2_COMPARE3/SAI2_TX_DATA/PWM8_OUT/GPIO1_IO15/REF_CLK_24M/CAAM_RNG_OSC_OBS
1473005-4
ETH_MDIO
ETH_MDC
LCD_BL_PWM
R92 0R TMS
R94 0R TDO
R95 0R TDI
R93 0R TCK
R96 0R TRSTn
R88 4k7
GND
J13B
liteSOM UART Group
UART1_TX_DATA K14 UART1_DCE_TX/UART1_DTE_RX/ENET1_RDATA02/I2C3_SCL/CSI_DATA02/GPT1_COMPARE1/GPIO1_IO16/SPDIF_OUT
UART1_RX_DATA K16 UART1_DCE_RX/UART1_DTE_TX/ENET1_RDATA03/I2C3_SDA/CSI_DATA03/GPT1_CLK/GPIO1_IO17/SPDIF_IN
UART1_CTS_B K15 UART1_DCE_CTS_B/UART1_DTE_RTS_B/ENET1_RX_CLK/USDHC1_WP/CSI_DATA04/ENET2_1588_EVENT1_IN/GPIO1_IO18/USDHC2_WP
UART1_RTS_B J14 UART1_DCE_RTS_B/UART1_DTE_CTS_B/ENET1_TX_ER/USDHC1_CD_B/CSI_DATA05/ENET2_1588_EVENT1_OUT/GPIO1_IO19/USDHC2_CD_B
UART2_TX_DATA J17 UART2_DCE_TX/UART2_DTE_RX/ENET1_TDATA02/I2C4_SCL/CSI_DATA06/GPT1_CAPTURE1/GPIO1_IO20/ECSPI3_SS0
UART2_RX_DATA J16 UART2_DCE_RX/UART2_DTE_TX/ENET1_TDATA03/I2C4_SDA/CSI_DATA07/GPT1_CAPTURE2/GPIO1_IO21/SJC_DONE/ECSPI3_SCLK
UART2_CTS_B J15 UART2_DCE_CTS_B/UART2_DTE_RTS_B/ENET1_CRS/FLEXCAN2_TX/CSI_DATA08/GPT1_COMPARE2/GPIO1_IO22/SJC_DE_B/ECSPI3_MOSI
UART2_RTS_B H14 UART2_DCE_RTS_B/UART2_DTE_CTS_B/ENET1_COL/FLEXCAN2_RX/CSI_DATA09/GPT1_COMPARE3/GPIO1_IO23/SJC_FAIL/ECSPI3_MISO
UART3_TX_DATA H17 UART3_DCE_TX/UART3_DTE_RX/ENET2_RDATA02/SIM1_PORT0_PD/CSI_DATA01/UART2_DCE_CTS_B/UART2_DTE_RTS_B/GPIO1_IO24/SJC_JTAG_ACT
UART3_RX_DATA H16 UART3_DCE_RX/UART3_DTE_TX/ENET2_RDATA03/SIM2_PORT0_PD/CSI_DATA00/UART2_DCE_RTS_B/UART2_DTE_CTS_B/GPIO1_IO25/EPIT1_OUT
UART3_CTS_B H15 UART3_DCE_CTS_B/UART3_DTE_RTS_B/ENET2_RX_CLK/FLEXCAN1_TX/CSI_DATA10/ENET1_1588_EVENT1_IN/GPIO1_IO26/EPIT2_OUT
UART3_RTS_B G14 UART3_DCE_RTS_B/UART3_DTE_CTS_B/ENET2_TX_ER/FLEXCAN1_RX/CSI_DATA11/ENET1_1588_EVENT1_OUT/GPIO1_IO27/WDOG1_WDOG_B
UART4_TX_DATA G17 UART4_DCE_TX/UART4_DTE_RX/ENET2_TDATA02/I2C1_SCL/CSI_DATA12/CSU_CSU_ALARM_AUT02/GPIO1_IO28/ECSPI2_SCLK
UART4_RX_DATA G16 UART4_DCE_RX/UART4_DTE_TX/ENET2_TDATA03/I2C1_SDA/CSI_DATA13/CSU_CSU_ALARM_AUT01/GPIO1_IO29/ECSPI2_SS0
UART5_TX_DATA F17 UART5_DCE_TX/UART5_DTE_RX/ENET2_CRS/I2C2_SCL/CSI_DATA14/CSU_CSU_ALARM_AUT00/GPIO1_IO30/ECSPI2_MOSI
UART5_RX_DATA G13 UART5_DCE_RX/UART5_DTE_TX/ENET2_COL/I2C2_SDA/CSI_DATA15/CSU_CSU_INT_DEB/GPIO1_IO31/ECSPI2_MISO
1473005-4
SD1_CDn
J13C
liteSOM ENET Group
ENET1_RX_DATA0 F16 ENET1_RDATA00/UART4_DCE_RTS_B/UART4_DTE_CTS_B/PWM1_OUT/CSI_DATA16/FLEXCAN1_TX/GPIO2_IO00/KPP_ROW00/USDHC1_LCTL
ENET1_RX_DATA1 E17 ENET1_RDATA01/UART4_DCE_CTS_B/UART4_DTE_RTS_B/PWM2_OUT/CSI_DATA17/FLEXCAN1_RX/GPIO2_IO01/KPP_COL00/USDHC2_LCTL
ENET1_RX_EN E16 ENET1_RX_EN/UART5_DCE_RTS_B/UART5_DTE_CTS_B/REF_CLK_32K/CSI_DATA18/FLEXCAN2_TX/GPIO2_IO02/KPP_ROW01/USDHC1_VSELECT
ENET1_TX_DATA0 E15 ENET1_TDATA00/UART5_DCE_CTS_B/UART5_DTE_RTS_B/REF_CLK_24M/CSI_DATA19/FLEXCAN2_RX/GPIO2_IO03/KPP_COL01/USDHC2_VSELECT
ENET1_TX_DATA1 E14 ENET1_TDATA01/UART6_DCE_CTS_B/UART6_DTE_RTS_B/PWM5_OUT/CSI_DATA20/ENET2_MDIO/GPIO2_IO04/KPP_ROW02/WDOG1_WDOG_RST_B_DEB
ENET1_TX_EN F15 ENET1_TX_EN/UART6_DCE_RTS_B/UART6_DTE_CTS_B/PWM6_OUT/CSI_DATA21/ENET2_MDC/GPIO2_IO05/KPP_COL02/WDOG2_WDOG_RST_B_DEB
ENET1_TX_CLK F14 ENET1_TX_CLK/UART7_DCE_CTS_B/UART7_DTE_RTS_B/PWM7_OUT/CSI_DATA22/ENET1_REF_CLK1/GPIO2_IO06/KPP_ROW03/GPT1_CLK
ENET1_RX_ER D15 ENET1_RX_ER/UART7_DCE_RTS_B/UART7_DTE_CTS_B/PWM8_OUT/CSI_DATA23/EIM_CRE/GPIO2_IO07/KPP_COL03/GPT1_CAPTURE2
ENET2_RX_DATA0 C17 ENET2_RDATA00/UART6_DCE_TX/UART6_DTE_RX/SIM1_PORT0_TRXD/I2C3_SCL/ENET1_MDIO/GPIO2_IO08/KPP_ROW04/USB_OTG1_PWR
ENET2_RX_DATA1 C16 ENET2_RDATA01/UART6_DCE_RX/UART6_DTE_TX/SIM1_PORT0_CLK/I2C3_SDA/ENET1_MDC/GPIO2_IO09/KPP_COL04/USB_OTG1_OC
ENET2_RX_EN B17 ENET2_RX_EN/UART7_DCE_TX/UART7_DTE_RX/SIM1_PORT0_RST_B/I2C4_SCL/EIM_ADDR26/GPIO2_IO10/KPP_ROW05/ENET1_REF_CLK_25M
ENET2_TX_DATA0 A15 ENET2_TDATA00/UART7_DCE_RX/UART7_DTE_TX/SIM1_PORT0_SVEN/I2C4_SDA/EIM_EB_B02/GPIO2_IO11/KPP_COL05/REF_CLK_24M
ENET2_TX_DATA1 A16 ENET2_TDATA01/UART8_DCE_TX/UART8_DTE_RX/SIM2_PORT0_TRXD/ECSPI4_SCLK/EIM_EB_B03/GPIO2_IO12/KPP_ROW06/USB_OTG2_PWR
ENET2_TX_EN B15 ENET2_TX_EN/UART8_DCE_RX/UART8_DTE_TX/SIM2_PORT0_CLK/ECSPI4_MOSI/EIM_ACLK_FREERUN/GPIO2_IO13/KPP_COL06/USB_OTG2_OC
ENET2_TX_CLK D17 ENET2_TX_CLK/UART8_DCE_CTS_B/UART8_DTE_RTS_B/SIM2_PORT0_RST_B/ECSPI4_MISO/ENET2_REF_CLK2/GPIO2_IO14/KPP_ROW07/ANATOP_OTG2_ID
ENET2_RX_ER D16 ENET2_RX_ER/UART8_DCE_RTS_B/UART8_DTE_CTS_B/SIM2_PORT0_SVEN/ECSPI4_SS0/EIM_ADDR25/GPIO2_IO15/KPP_COL07/WDOG1_WDOG_ANY
1473005-4
USB1_PWR
J13D
liteSOM SD1 Group
SD1_CMD C2 USDHC1_CMD/GPT2_COMPARE1/SAI2_RX_SYNC/SPDIF_OUT/EIM_ADDR19/GPIO2_IO16/SDMA_EXT_EVENT00/USB_OTG1_PWR
SD1_CLK C1 USDHC1_CLK/GPT2_COMPARE2/SAI2_MCLK/SPDIF_IN/EIM_ADDR20/GPIO2_IO17/USB_OTG1_OC
SD1_DATA0 B3 USDHC1_DATA0/GPT2_COMPARE3/SAI2_TX_SYNC/FLEXCAN1_TX/EIM_ADDR21/GPIO2_IO18/ANATOP_OTG1_ID
SD1_DATA1 B2 USDHC1_DATA1/GPT2_CLK/SAI2_TX_BCLK/FLEXCAN1_RX/EIM_ADDR22/GPIO2_IO19/USB_OTG2_PWR
SD1_DATA2 B1 USDHC1_DATA2/GPT2_CAPTURE1/SAI2_RX_DATA/FLEXCAN2_TX/EIM_ADDR23/GPIO2_IO20/CCM_CLKO1/USB_OTG2_OC
SD1_DATA3 A2 USDHC1_DATA3/GPT2_CAPTURE2/SAI2_TX_DATA/FLEXCAN2_RX/EIM_ADDR24/GPIO2_IO21/CCM_CLKO2/ANATOP_OTG2
1473005-4
SD1_CMD
SD1_CLK
SD1_DATA0
SD1_DATA1
SD1_DATA2
SD1_DATA3
SD1_DATA[3..0]
3V3
J14
TMS
TCK
TDO
TDI
TRSTn
GND
JTAG
623310235521
Warning!
For unknown reason
CTS/RTS ports direction are
swapped in the i.MX6UL
documentation.
UARTx_CTS_B is output
and UARTx_RTS_B is input.
This is in oposite to
commony used naming
convention.
Title liteSOM part 1
Size A4
Project liteboard
Rev 1.3.0
Date 2017-11-24
Number *
Sheet 2 / 8
GRINN
DESIGN HOUSE OF ELECTRONICS


J13E
liteSOM LCD Group
LCD_CLK A8 LCDIF_CLK/LCDIF_WR_RWN/UART4_DCE_TX/UART4_DTE_RX/SAI3_MCLK/EIM_CS2_B/GPIO3_IO00/WDOG1_WDOG_RST_B_DEB
LCD_ENABLE B8 LCDIF_ENABLE/LCDIF_RD_E/UART4_DCE_RX/UART4_DTE_TX/SAI3_TX_SYNC/EIM_CS3_B/GPIO3_IO01/ECSPI2_RDY
LCD_HSYNC D9 LCDIF_HSYNC/LCDIF_RS/UART4_DCE_CTS_B/UART4_DTE_RTS_B/SAI3_TX_BCLK/WDOG3_WDOG_RST_B_DEB/GPIO3_IO02/ECSPI2_SS1
LCD_VSYNC C9 LCDIF_VSYNC/LCDIF_BUSY/UART4_DCE_RTS_B/UART4_DTE_CTS_B/SAI3_RX_DATA/WDOG2_WDOG_B/GPIO3_IO03/ECSPI2_SS2
LCD_RESET E9 LCDIF_RESET/LCDIF_CS/CA7_MX6UL_EVENTI/SAI3_TX_DATA/WDOG1_WDOG_ANY/GPIO3_IO04/ECSPI2_SS3
LCD_DATA00 B9 LCDIF_DATA00/PWM1_OUT/CA7_MX6UL_TRACE0/ENET1_1588_EVENT2_IN/I2C3_SDA/GPIO3_IO05/SRC_BT_CFG00/SAI1_MCLK
LCD_DATA01 A9 LCDIF_DATA01/PWM2_OUT/CA7_MX6UL_TRACE1/ENET1_1588_EVENT2_OUT/I2C3_SCL/GPIO3_IO06/SAI1_TX_SYNC
LCD_DATA02 E10 LCDIF_DATA02/PWM3_OUT/CA7_MX6UL_TRACE2/ENET1_1588_EVENT3_IN/I2C4_SDA/GPIO3_IO07/SRC_BT_CFG02/SAI1_TX_BCLK
LCD_DATA03 D10 LCDIF_DATA03/PWM4_OUT/CA7_MX6UL_TRACE3/ENET1_1588_EVENT3_OUT/I2C4_SCL/GPIO3_IO08/SRC_BT_CFG03/SAI1_RX_DATA
LCD_DATA04 C10 LCDIF_DATA04/UART8_DCE_CTS_B/UART8_DTE_RTS_B/CA7_MX6UL_TRACE4/ENET2_1588_EVENT2_IN/SPDIF_SR_CLK/GPIO3_IO09/SRC_BT_CFG04/SAI1_TX_DATA
LCD_DATA05 B10 LCDIF_DATA05/UART8_DCE_RTS_B/UART8_DTE_CTS_B/CA7_MX6UL_TRACE5/ENET2_1588_EVENT2_OUT/SPDIF_OUT/GPIO3_IO10/SRC_BT_CFG05/ECSPI1_SS1
LCD_DATA06 A10 LCDIF_DATA06/UART7_DCE_CTS_B/UART7_DTE_RTS_B/CA7_MX6UL_TRACE6/ENET2_1588_EVENT3_IN/SPDIF_LOCK/GPIO3_IO11/SRC_BT_CFG06/ECSPI1_SS2
LCD_DATA07 D11 LCDIF_DATA07/UART7_DCE_RTS_B/UART7_DTE_CTS_B/CA7_MX6UL_TRACE7/ENET2_1588_EVENT3_OUT/SPDIF_EXT_CLK/GPIO3_IO12/SRC_BT_CFG07/ECSPI1_SS3
LCD_DATA08 B11 LCDIF_DATA08/SPDIF_IN/CA7_MX6UL_TRACE8/CSI_DATA16/EIM_DATA00/GPIO3_IO13/SRC_BT_CFG08/FLEXCAN1_TX
LCD_DATA09 A11 LCDIF_DATA09/SAI3_MCLK/CA7_MX6UL_TRACE9/CSI_DATA17/EIM_DATA01/GPIO3_IO14/SRC_BT_CFG09/FLEXCAN1_RX
LCD_DATA10 E12 LCDIF_DATA10/SAI3_RX_SYNC/CA7_MX6UL_TRACE10/CSI_DATA18/EIM_DATA02/GPIO3_IO15/SRC_BT_CFG10/FLEXCAN2_TX
LCD_DATA11 D12 LCDIF_DATA11/SAI3_RX_BCLK/CA7_MX6UL_TRACE11/CSI_DATA19/EIM_DATA03/GPIO3_IO16/SRC_BT_CFG11/FLEXCAN2_RX
LCD_DATA12 C12 LCDIF_DATA12/SAI3_TX_SYNC/CA7_MX6UL_TRACE12/CSI_DATA20/EIM_DATA04/GPIO3_IO17/SRC_BT_CFG12/ECSPI1_RDY
LCD_DATA13 B12 LCDIF_DATA13/SAI3_TX_BCLK/CA7_MX6UL_TRACE13/CSI_DATA21/EIM_DATA05/GPIO3_IO18/SRC_BT_CFG13/USDHC2_RESET_B
LCD_DATA14 A12 LCDIF_DATA14/SAI3_RX_DATA/CA7_MX6UL_TRACE14/CSI_DATA22/EIM_DATA06/GPIO3_IO19/SRC_BT_CFG14/USDHC2_DATA4
LCD_DATA15 D13 LCDIF_DATA15/SAI3_TX_DATA/CA7_MX6UL_TRACE15/CSI_DATA23/EIM_DATA07/GPIO3_IO20/SRC_BT_CFG15/USDHC2_DATA5
LCD_DATA16 C13 LCDIF_DATA16/UART7_DCE_TX/UART7_DTE_RX/CA7_MX6UL_TRACE_CLK/CSI_DATA01/EIM_DATA08/GPIO3_IO21/SRC_BT_CFG24/USDHC2_DATA6
LCD_DATA17 B13 LCDIF_DATA17/UART7_DCE_RX/UART7_DTE_TX/CA7_MX6UL_TRACE_CTL/CSI_DATA00/EIM_DATA09/GPIO3_IO22/SRC_BT_CFG25/USDHC2_DATA7
LCD_DATA18 A13 LCDIF_DATA18/PWM5_OUT/CA7_MX6UL_EVENTO/CSI_DATA10/EIM_DATA10/GPIO3_IO23/SRC_BT_CFG26/USDHC2_CMD
LCD_DATA19 D14 LCDIF_DATA19/PWM6_OUT/WDOG1_WDOG_ANY/CSI_DATA11/EIM_DATA11/GPIO3_IO24/SRC_BT_CFG27/USDHC2_CLK
LCD_DATA20 C14 LCDIF_DATA20/UART8_DCE_TX/UART8_DTE_RX/ECSPI1_SCLK/CSI_DATA12/EIM_DATA12/GPIO3_IO25/SRC_BT_CFG28/USDHC2_DATA0
LCD_DATA21 B14 LCDIF_DATA21/UART8_DCE_RX/UART8_DTE_TX/ECSPI1_SS0/CSI_DATA13/EIM_DATA13/GPIO3_IO26/SRC_BT_CFG29/USDHC2_DATA1
LCD_DATA22 A14 LCDIF_DATA22/MQS_RIGHT/ECSPI1_MOSI/CSI_DATA14/EIM_DATA14/GPIO3_IO27/SRC_BT_CFG30/USDHC2_DATA2
LCD_DATA23 B16 LCDIF_DATA23/MQS_LEFT/ECSPI1_MISO/CSI_DATA15/EIM_DATA15/GPIO3_IO28/SRC_BT_CFG31/USDHC2_DATA3
1473005-4
BOOT_CFG1_0
BOOT_CFG1_1
BOOT_CFG1_2
BOOT_CFG1_3
BOOT_CFG1_4
BOOT_CFG1_5
BOOT_CFG1_6
BOOT_CFG1_7
BOOT_CFG2_0
BOOT_CFG2_1
BOOT_CFG2_2
BOOT_CFG2_3
BOOT_CFG2_4
BOOT_CFG2_5
BOOT_CFG2_6
BOOT_CFG2_7
BOOT_CFG4_0
BOOT_CFG4_1
BOOT_CFG4_2
BOOT_CFG4_3
BOOT_CFG4_4
BOOT_CFG4_5
BOOT_CFG4_6
BOOT_CFG4_7
J13H
liteSOM SNVS Group
SNVS_TAMPER0 R10 GPIO5_IO00
SNVS_TAMPER1 R9 GPIO5_IO01
SNVS_TAMPER2 P11 GPIO5_IO02
SNVS_TAMPER3 P10 GPIO5_IO03
SNVS_TAMPER4 P9 GPIO5_IO04
SNVS_TAMPER5 N8 GPIO5_IO05
SNVS_TAMPER6 N11 GPIO5_IO06
SNVS_TAMPER7 N10 GPIO5_IO07
SNVS_TAMPER8 N9 GPIO5_IO08
SNVS_TAMPER9 R6 GPIO5_IO09
ONOFF R8
POR_B P8
BOOT_MODE0 T10
BOOT_MODE1 U10
PMIC_STBY_REQ U9
PMIC_ON_REQ T9
BMODE0
BMODE1
TP2
1473005-4
BOOT_CFG2[6] BOOT_CFG2[5] BOOT_CFG2[3] BOOT_CFG1[5] BMODE1 BMODE0
X X X X 0 0 Boot From Fuses
X X X X 0 1 Serial Downloader
0 0 0 0 1 0 SDHC1 1-bit
0 1 0 0 1 0 SDHC1 4-bit
0 0 1 1 1 0 eMMC2 1-bit
0 1 1 1 1 0 eMMC2 4-bit
1 0 1 1 1 0 eMMC2 8-bit
3V3
3V3_SNVS
R100 R99 R98 R97 R4 R5
S1
R52
BMODE1
BMODE0
GND
3V3
R90 4k7
R91 4k7
J13G
liteSOM CSI Group
CSI_MCLK F5 CSI_MCLK/USDHC2_CD_B/RAWNAND_CE2_B/I2C1_SDA/EIM_CS0_B/GPIO4_IO17/SNVS_HP_VIO_5_CTL/UART6_DCE_TX/UART6_DTE_RX
CSI_PIXCLK E5 CSI_PIXCLK/USDHC2_WP/RAWNAND_CE3_B/I2C1_SCL/EIM_OE/GPIO4_IO18/SNVS_HP_VIO_5/UART6_DCE_RX/UART6_DTE_TX
CSI_VSYNC F2 CSI_VSYNC/USDHC2_CLK/SIM1_PORT1_CLK/I2C2_SDA/EIM_RW/GPIO4_IO19/PWM7_OUT/UART6_DCE_RTS_B/UART6_DTE_CTS_B
CSI_HSYNC F3 CSI_HSYNC/USDHC2_CMD/SIM1_PORT1_PD/I2C2_SCL/EIM_LBA_B/GPIO4_IO20/PWM8_OUT/UART6_DCE_CTS_B/UART6_DTE_RTS_B
CSI_DATA00 E4 CSI_DATA02/USDHC2_DATA0/SIM1_PORT1_RST_B/ECSPI2_SCLK/EIM_AD00/GPIO4_IO21/SRC_INT_BOOT/UART5_DCE_TX/UART5_DTE_RX
CSI_DATA01 E3 CSI_DATA03/USDHC2_DATA1/SIM1_PORT1_SVEN/ECSPI2_SS0/EIM_AD01/GPIO4_IO22/SAI1_MCLK/UART5_DCE_RX/UART5_DTE_TX
CSI_DATA02 E2 CSI_DATA04/USDHC2_DATA2/SIM1_PORT1_TRXD/ECSPI2_MOSI/EIM_AD02/GPIO4_IO23/SAI1_RX_SYNC/UART5_DCE_RTS_B/UART5_DTE_CTS_B
CSI_DATA03 E1 CSI_DATA05/USDHC2_DATA3/SIM2_PORT1_PD/ECSPI2_MISO/EIM_AD03/GPIO4_IO24/SAI1_RX_BCLK/UART5_DCE_CTS_B/UART5_DTE_RTS_B
CSI_DATA04 D4 CSI_DATA06/USDHC2_DATA4/SIM2_PORT1_CLK/ECSPI1_SCLK/EIM_AD04/GPIO4_IO25/SAI1_TX_SYNC/USDHC1_WP
CSI_DATA05 D3 CSI_DATA07/USDHC2_DATA5/SIM2_PORT1_RST_B/ECSPI1_SS0/EIM_AD05/GPIO4_IO26/SAI1_TX_BCLK/USDHC1_CD_B
CSI_DATA06 D2 CSI_DATA08/USDHC2_DATA6/SIM2_PORT1_SVEN/ECSPI1_MOSI/EIM_AD06/GPIO4_IO27/SAI1_RX_DATA/USDHC1_RESET_B
CSI_DATA07 D1 CSI_DATA09/USDHC2_DATA7/SIM2_PORT1_TRXD/ECSPI1_MISO/EIM_AD07/GPIO4_IO28/SAI1_TX_DATA/USDHC1_VSELECT
1473005-4
J13F
liteSOM NAND Group
NAND_WP_B D5 RAWNAND_WP_B/USDHC1_RESET_B/QSPI_A_SCLK/PWM4_OUT/EIM_BCLK/GPIO4_IO11/ECSPI3_RDY
NAND_READY_B A3 RAWNAND_READY_B/USDHC1_DATA4/QSPI_A_DATA00/ECSPI3_SS0/EIM_CS1_B/GPIO4_IO12/UART3_DCE_TX/UART3_DTE_RX
NAND_CE0_B C5 RAWNAND_CE0_B/USDHC1_DATA5/QSPI_A_DATA01/ECSPI3_SCLK/EIM_DTACK_B/GPIO4_IO13/UART3_DCE_RX/UART3_DTE_TX
NAND_CE1_B B5 RAWNAND_CE1_B/USDHC1_DATA6/QSPI_A_DATA02/ECSPI3_MOSI/EIM_ADDR18/GPIO4_IO14/UART3_DCE_CTS_B/UART3_DTE_RTS_B
NAND_CLE A4 RAWNAND_CLE/USDHC1_DATA7/QSPI_A_DATA03/ECSPI3_MISO/EIM_ADDR16/GPIO4_IO15/UART3_DCE_RTS_B/UART3_DTE_CTS_B
NAND_DQS E6 RAWNAND_DQS/CSI_FIELD/QSPI_A_SS0_B/PWM5_OUT/EIM_WAIT/GPIO4_IO16/SDMA_EXT_EVENT01/SPDIF_EXT_CLK
1473005-4
BOOT_CFG4_7 BOOT_CFG4_6 BOOT_CFG4_5 BOOT_CFG4_4 BOOT_CFG4_3 BOOT_CFG4_2 BOOT_CFG4_1 BOOT_CFG4_0 BOOT_CFG2_7 BOOT_CFG2_6 BOOT_CFG2_5 BOOT_CFG2_4 BOOT_CFG2_3 BOOT_CFG2_2 BOOT_CFG2_1 BOOT_CFG2_0 BOOT_CFG1_7 BOOT_CFG1_6 BOOT_CFG1_5 BOOT_CFG1_4 BOOT_CFG1_3 BOOT_CFG1_2 BOOT_CFG1_1 BOOT_CFG1_0
R87 R86 R85 R84 R83 R82 R81 R80 R79 R78 R77 R76 R75 R74 R73 R72 R71 R66 R64 R62 R61 R60 R59
J13I
liteSOM USB
USB_OTG1_DP U15
USB_OTG1_DN T15
USB_OTG1_VBUS T12
USB_OTG1_CHD_B U16
USB_OTG2_DP U13
USB_OTG2_DN T13
USB_OTG2_VBUS U12
1473005-4
USB_OTG1_D_P
USB_OTG1_D_N
USB_OTG1_VBUS
USB_OTG2_D_P
USB_OTG2_D_N
USB_OTG2_VBUS
USB2_D_P
USB2_D_N
TP3
90ohm_diff
J13J
liteSOM CCM
CCM_CLK1_P P17
CCM_CLK1_N P16
1473005-4
CCM_CLK1_P
CCM_CLK1_N
100ohm_diff
Title liteSOM part 2
Size A4
Project liteboard
Rev 1.3.0
Date 2017-11-24
Number *
Sheet 3 / 8
GRINN
DESIGN HOUSE OF ELECTRONICS



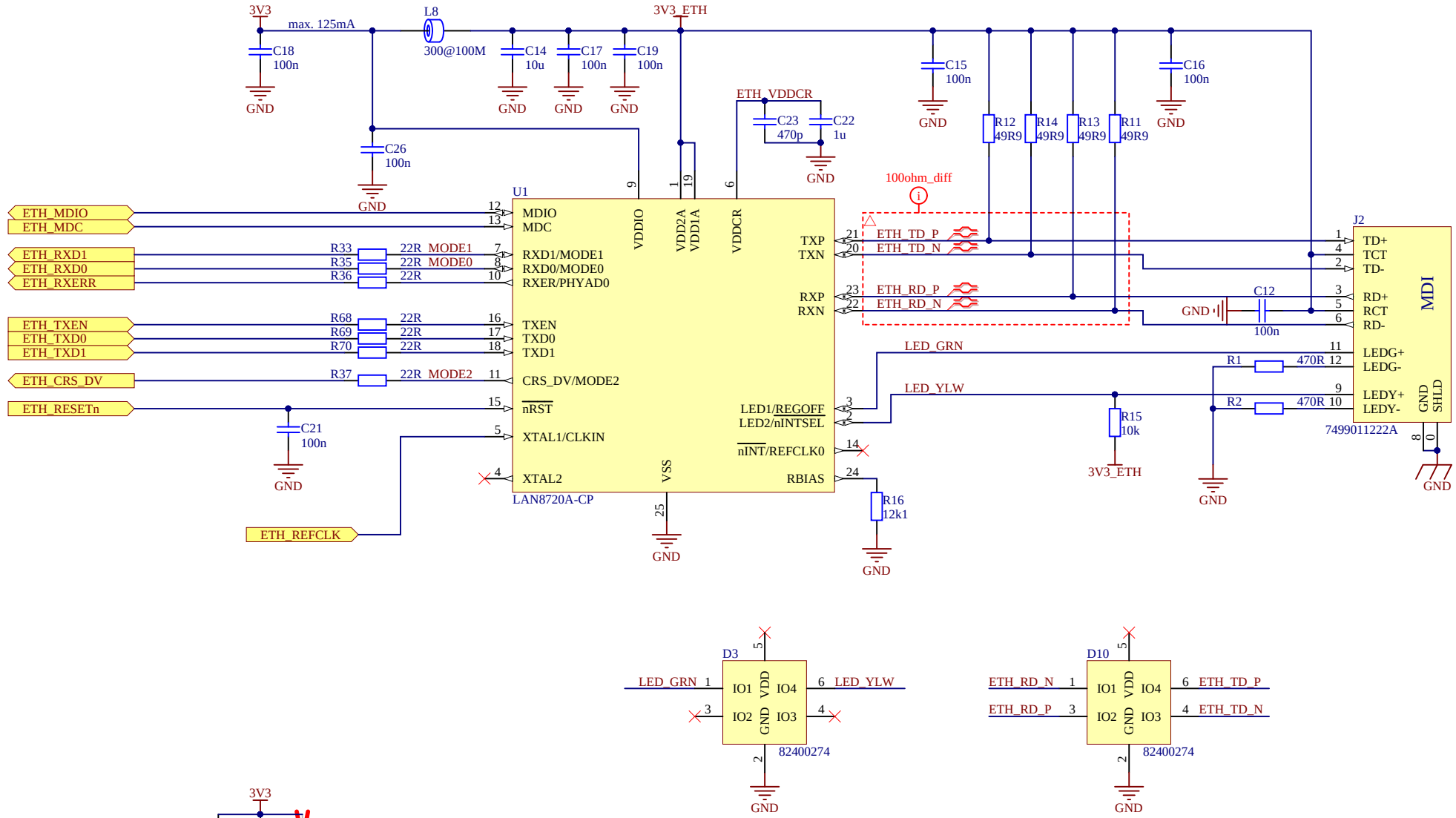
Title	liteSOM part 3		
Size	A4	Project liteboard	Rev 1.3.0
Date	2017-11-24	Number *	Sheet 4 / 8

GRINN
DESIGN HOUSE OF ELECTRONICS



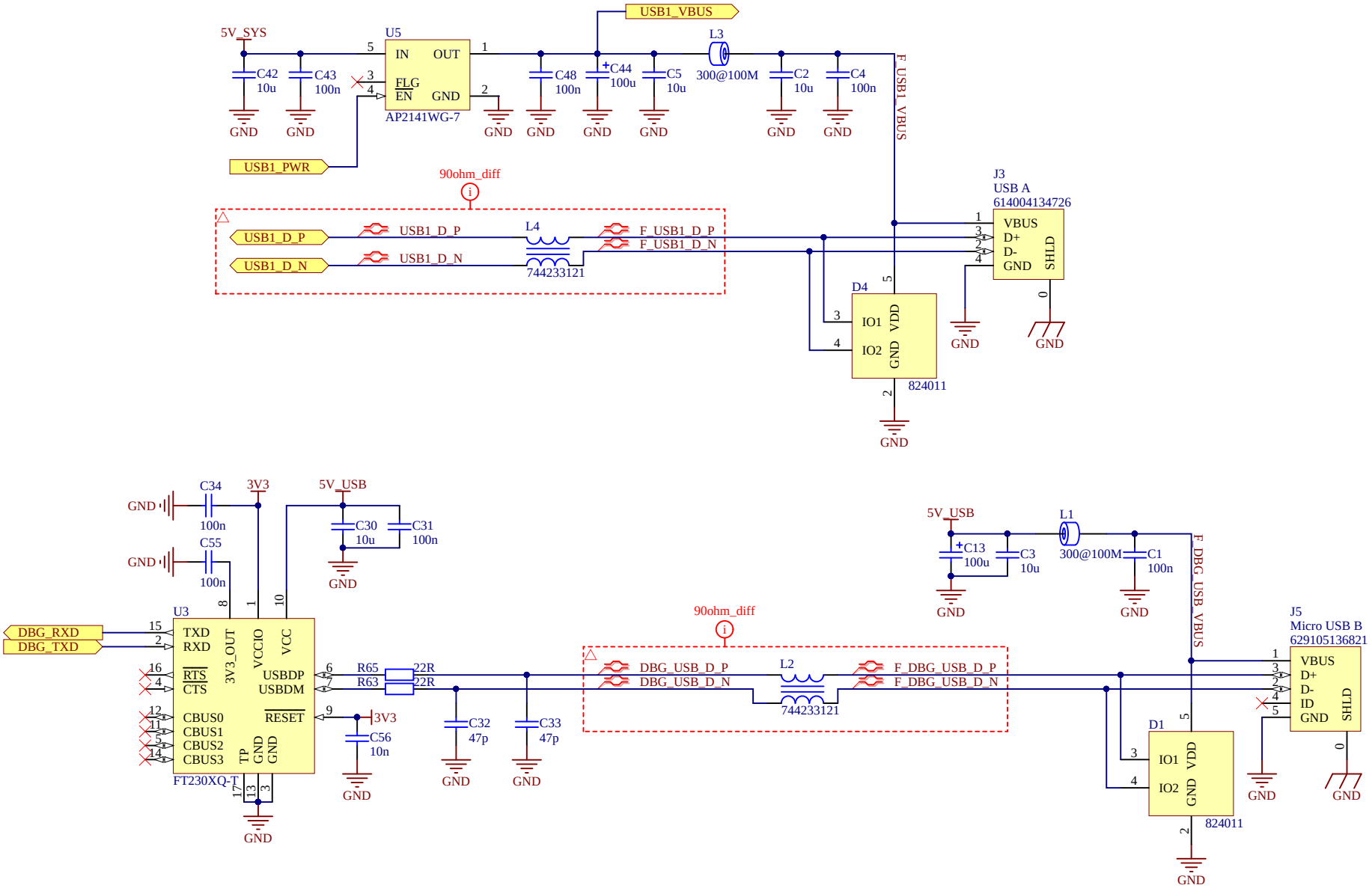
Title	Micro SD Card Socket		
Size	A4	Project liteboard	Rev 1.3.0
Date	2017-11-24	Number	Sheet 5 / 8

GRINN
DESIGN HOUSE OF ELECTRONICS



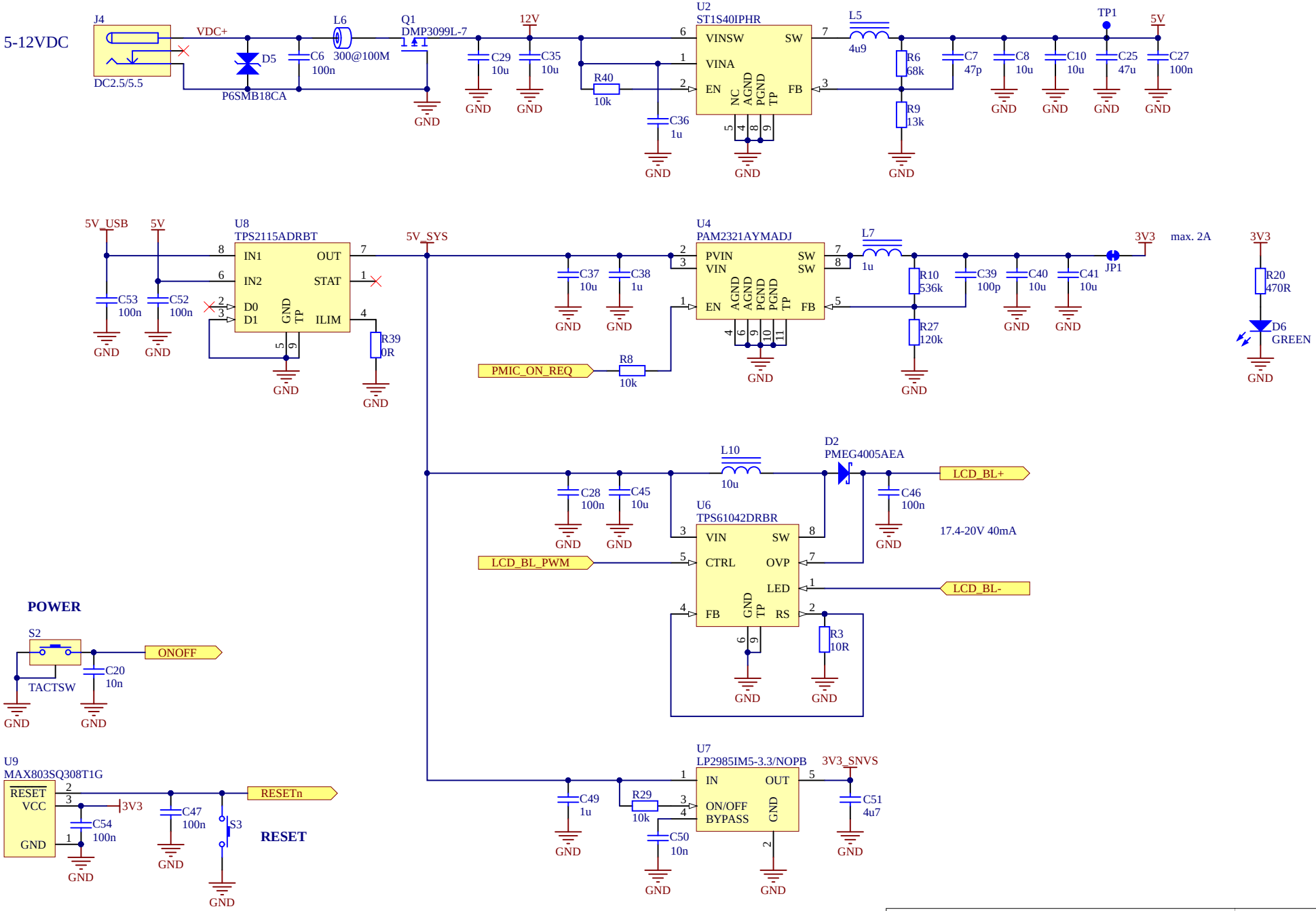
Title	Ethernet PHY		
Size	A4	Project liteboard	Rev 1.3.0
Date	2017-11-24	Number *	Sheet 6 / 8

GRINN
DESIGN HOUSE OF ELECTRONICS



Title	USB		
Size	A4	Project liteboard	Rev 1.3.0
Date	2017-11-24	Number *	Sheet 7 / 8

GRINN
DESIGN HOUSE OF ELECTRONICS



Title	Power Supply and Reset		
Size	A4	Project liteboard	Rev 1.3.0
Date	2017-11-24	Number *	Sheet 8 / 8

GRINN
DESIGN HOUSE OF ELECTRONICS