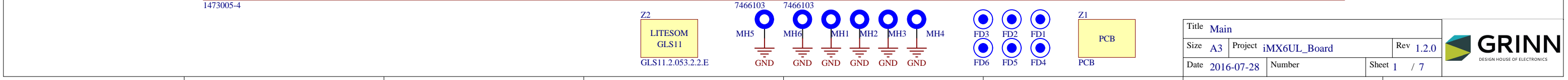
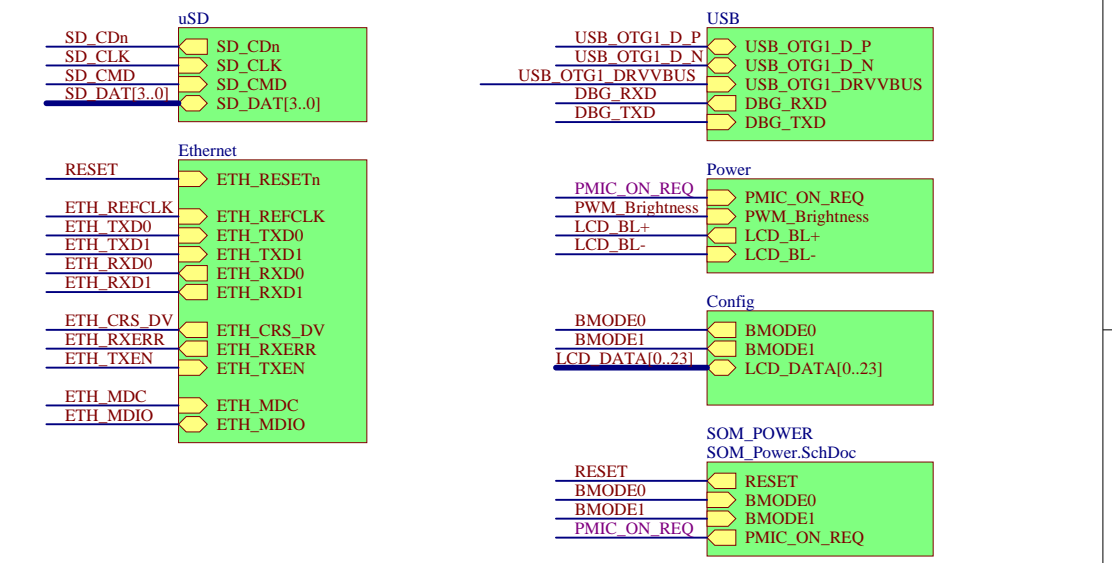
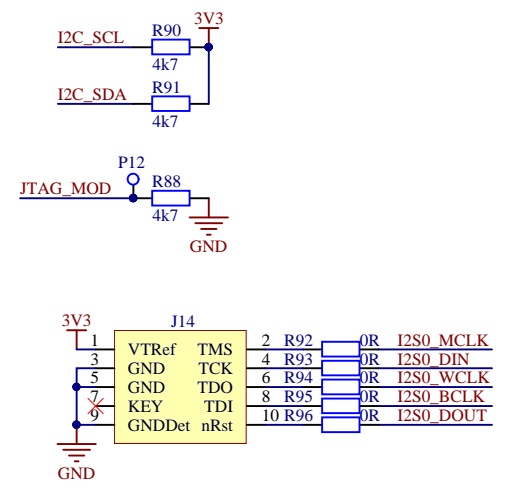
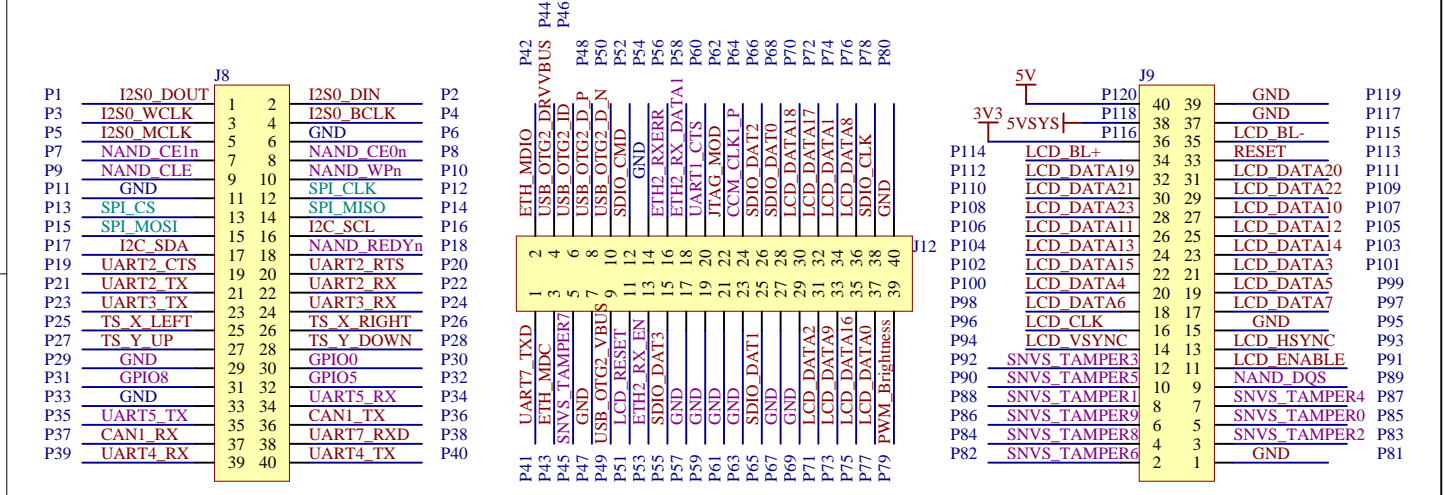
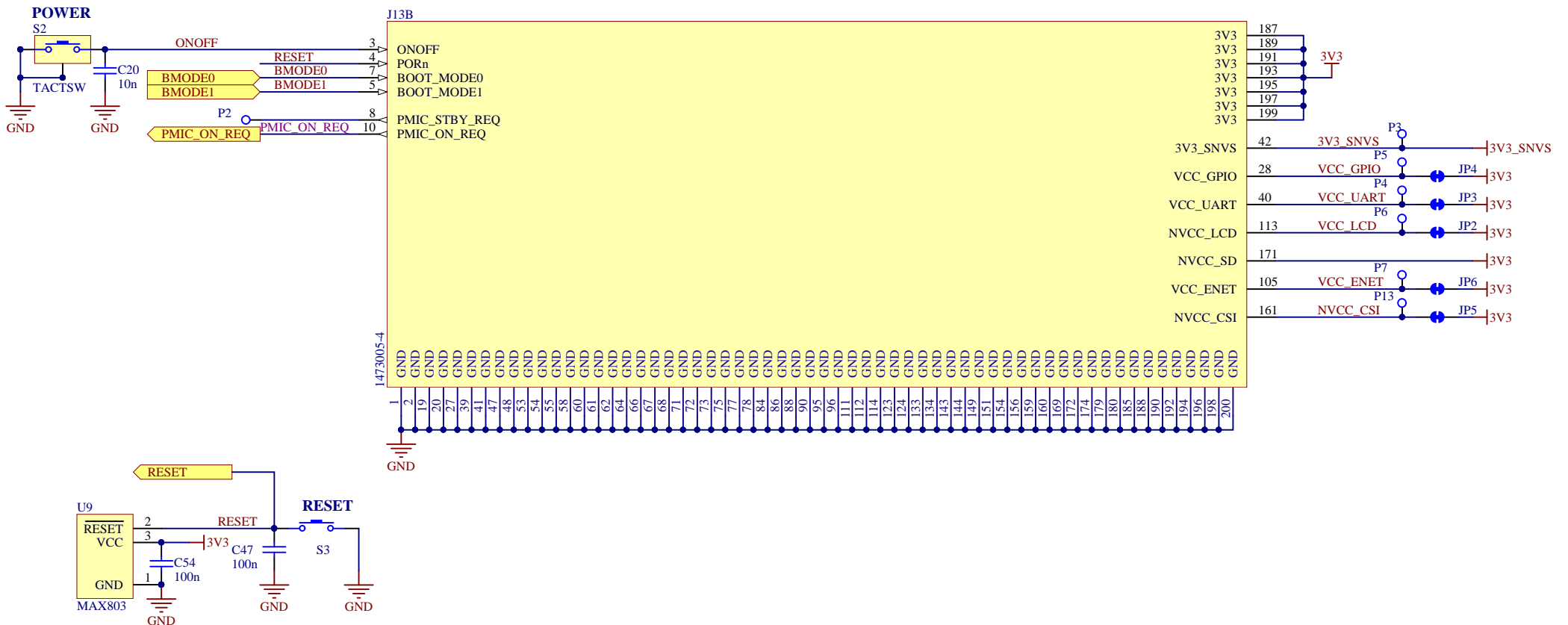


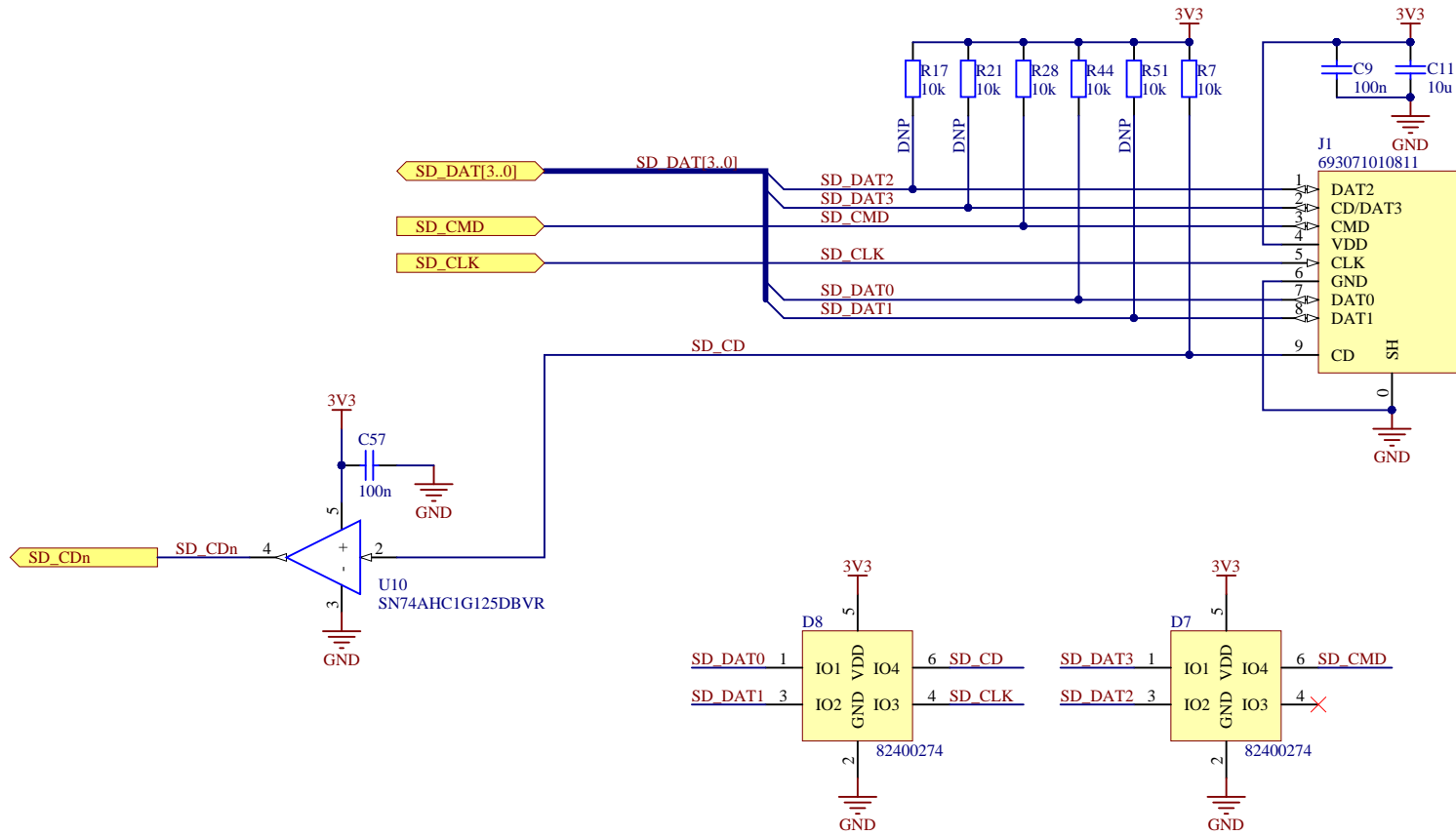
ChiliBoard Sandwich Connectors





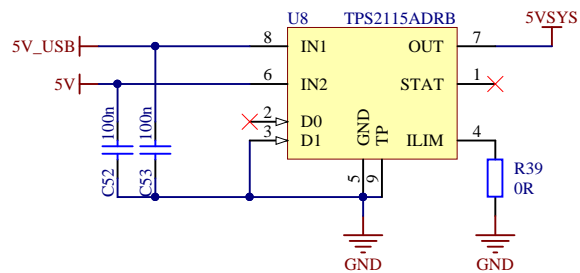
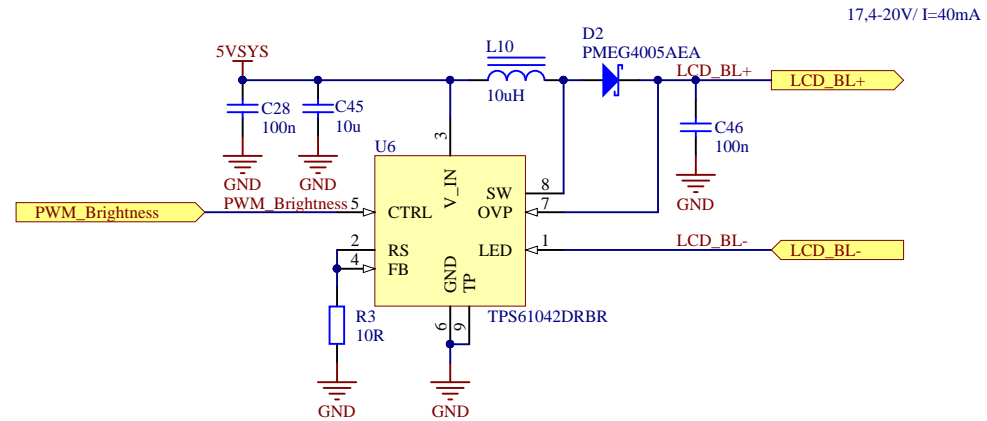
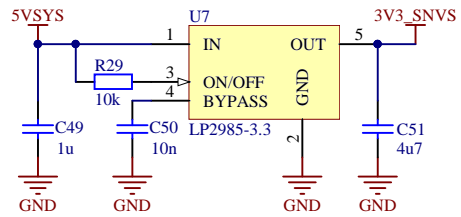
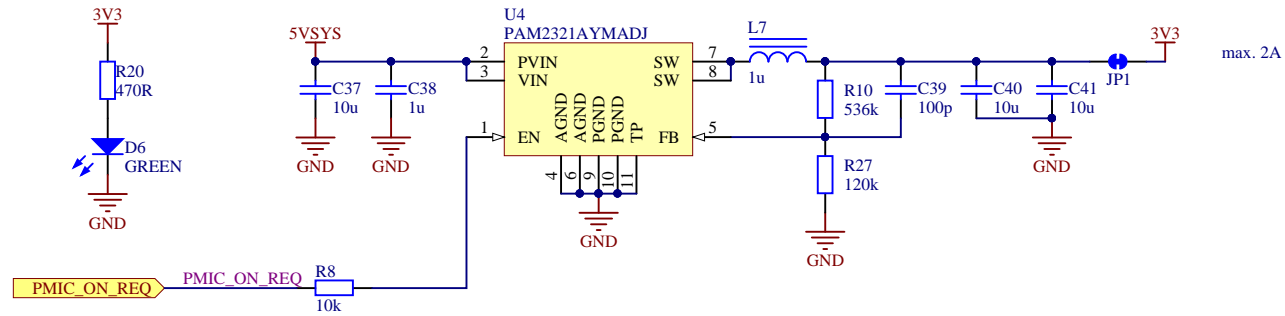
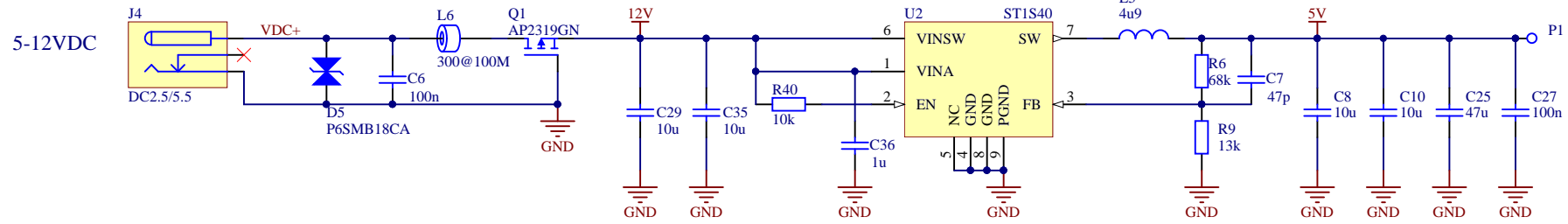
Title SOM Power		Rev 1.2.0	
Size A4	Project iMX6UL_Board		
Date 2016-07-28	Number	Sheet 2 / 7	





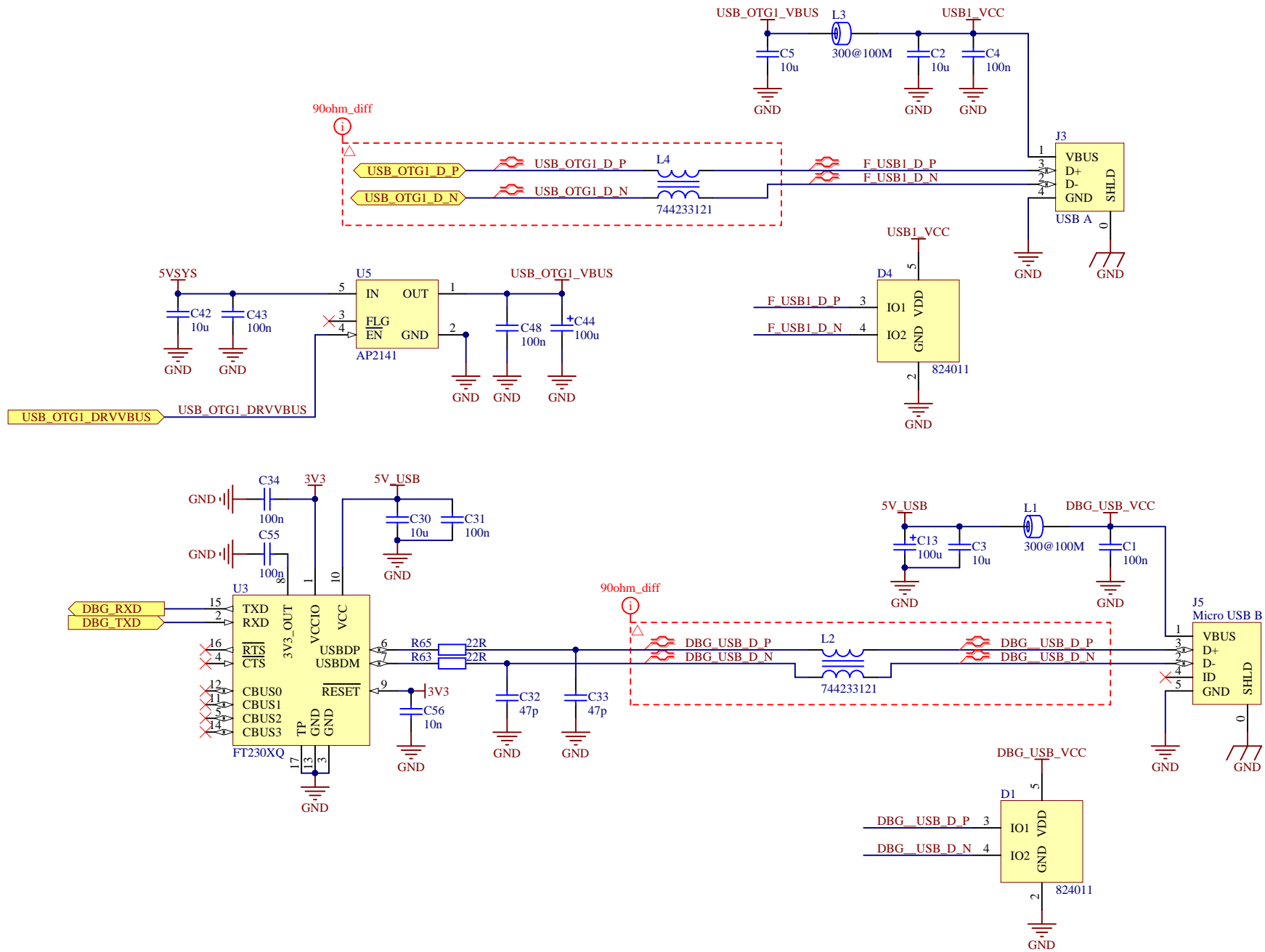
Title		Micro SD Card Socket	
Size	A4	Project	iMX6UL_Board
Date	2016-07-28	Rev	1.2.0
		Number	
		Sheet	3 / 7





Title		Power Supply	
Size	A4	Project	iMX6UL_Board
Date	2016-07-28	Rev	1.2.0
	Number *	Sheet	4 / 7





Title USB			
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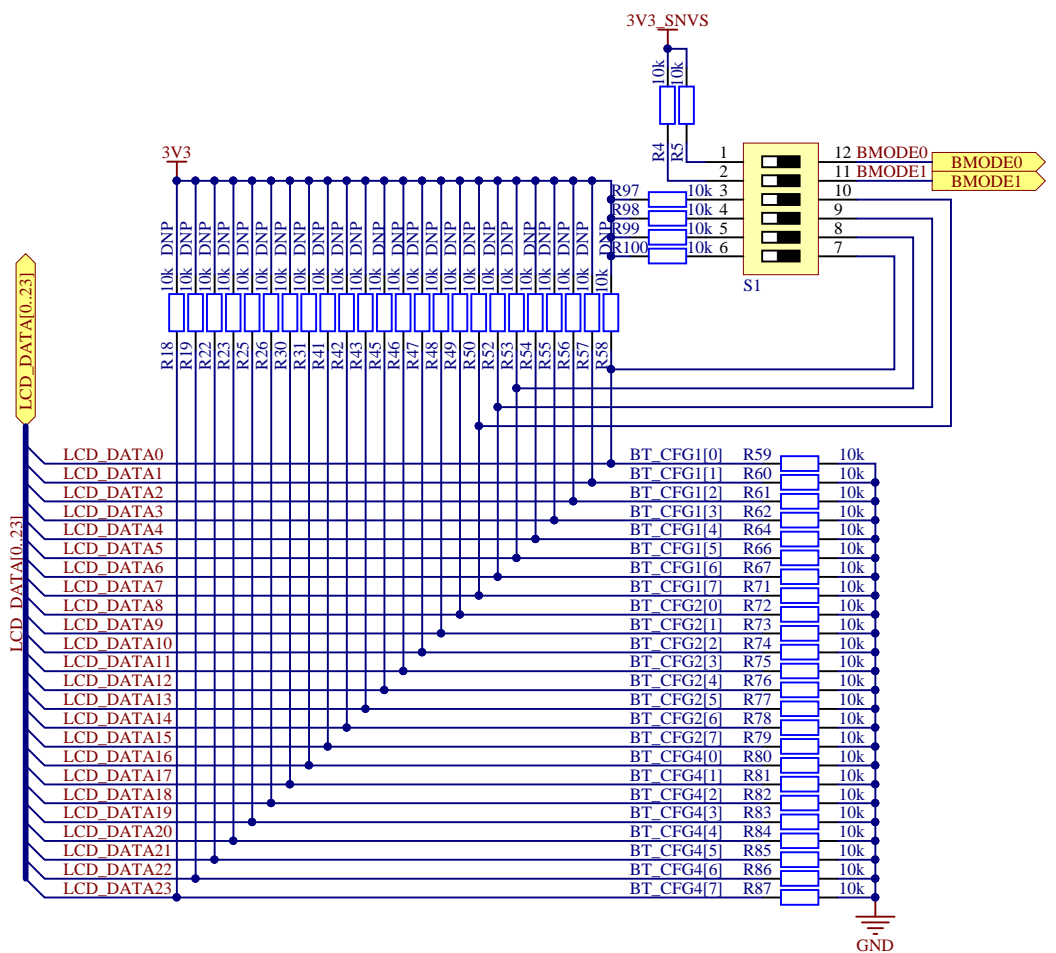
FUSE MAP

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved			DDRSMPL: "000" - Default "001-111"
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/GPIO Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	SD Power Cycle Enable: 0 - No power cycle 1 - Enabled via USDPHC_RST pad (USDPHC2 & 4 only)	SD Loopback Clock Source: 0 - through SD pad 1 - direct	SD Loopback Clock Source: 0 - through SD pad 1 - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed: 0 - High 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable: 0 - No power cycle 1 - Enabled via USDPHC_RST pad (USDPHC2 & 4 only)	SD Loopback Clock Source: 0 - through SD pad 1 - direct
NAND	1	BT_TOGGLEMODE	Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand Row address bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	SDHS: Half Speed Phase Selection: 0 - Speed sampling at reset/enable delay 1 - Full speed delay	SDHS: Half Speed Delay: 0 - Disabled delay 1 - Full speed delay	SDHS: Full Speed Phase Selection: 0 - Speed sampling at reset/enable delay 1 - Full speed delay	SDHS: Full Speed Delay: 0 - Disabled delay 1 - Full speed delay	Boot Frequencies (ARM/DSP): 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Musing Scheme: 00 - A/D16 01 - A/D8 10 - A/D4 11 - Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved	Reserved	Reserved	Boot Frequencies (ARM/DSP): 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DSP): 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step: 00 - 1 TBD	Bus Width: 0 - 1-bit 1 - 4-bit		Pre-Select: 00 - ASDMC1 01 - ASDMC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DSP): 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	Reserved	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Etc - reserved			Pre-Select: 00 - ASDMC1 01 - ASDMC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DSP): 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	Reserved	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: 000 - 16 SPI/CPLX cycles 001 - 8 SPI/CPLX cycles 010 - 4 SPI/CPLX cycles 011 - 2 SPI/CPLX cycles 100 - 4 SPI/CPLX cycles 101 - 2 SPI/CPLX cycles 110 - 6 SPI/CPLX cycles 111 - 7 SPI/CPLX cycles			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8	Boot Frequencies (ARM/DSP): 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time: 0 - 12ms 1 - 220ms (48A Nand)	Reserved	Reserved

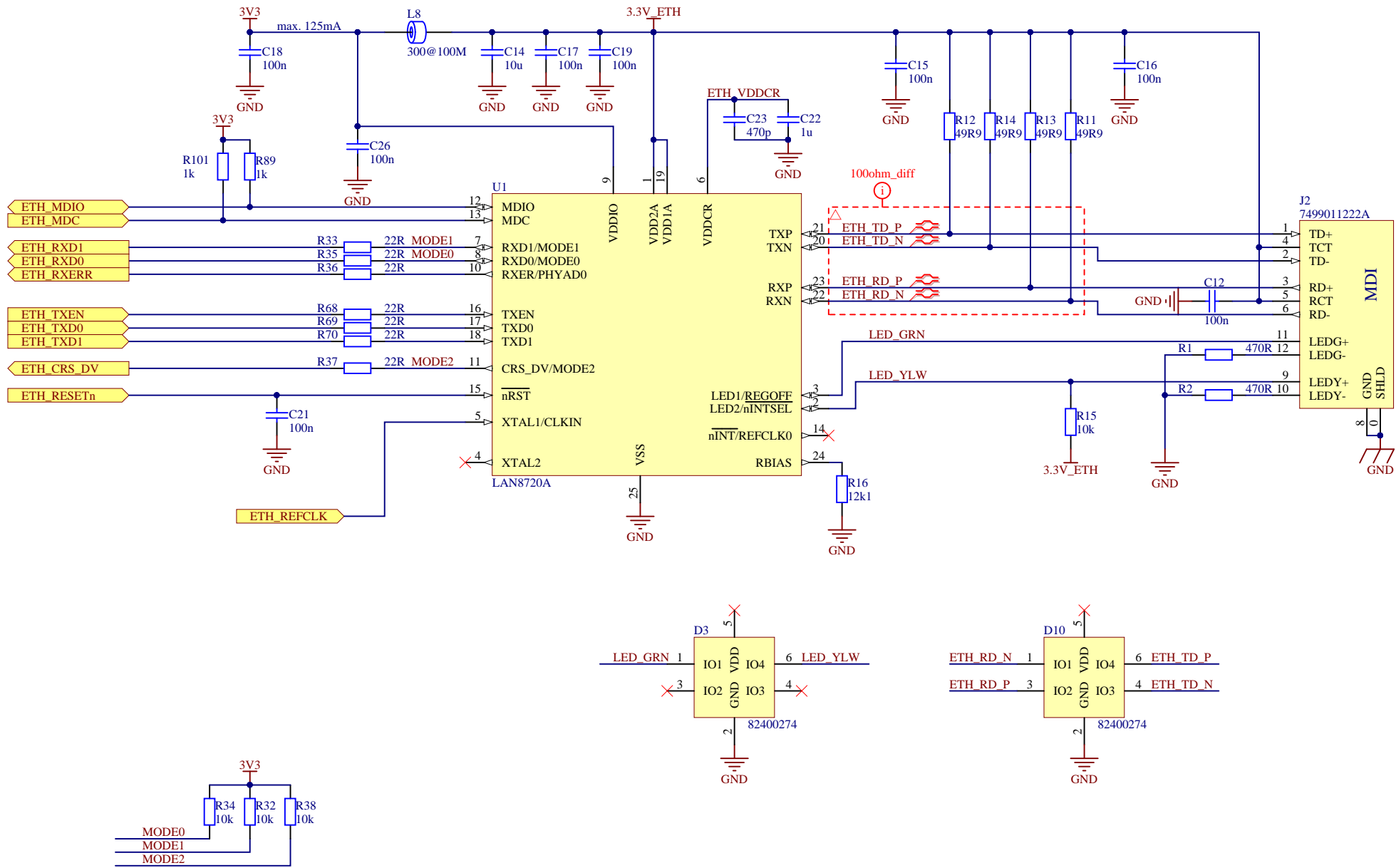
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinite-Loop (Debug USE only): 0 - Disable 1 - Enable	EEPROM Recovery Enable: 0 - Disabled 1 - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3	SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)			Flash Select: 000 - eCS#1 001 - eCS#2 010 - eCS#3 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDG_ENABLE: 0 - Disabled 1 - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE: 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC

dość switch na CFG2[4] i CFG2[5]



BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved





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