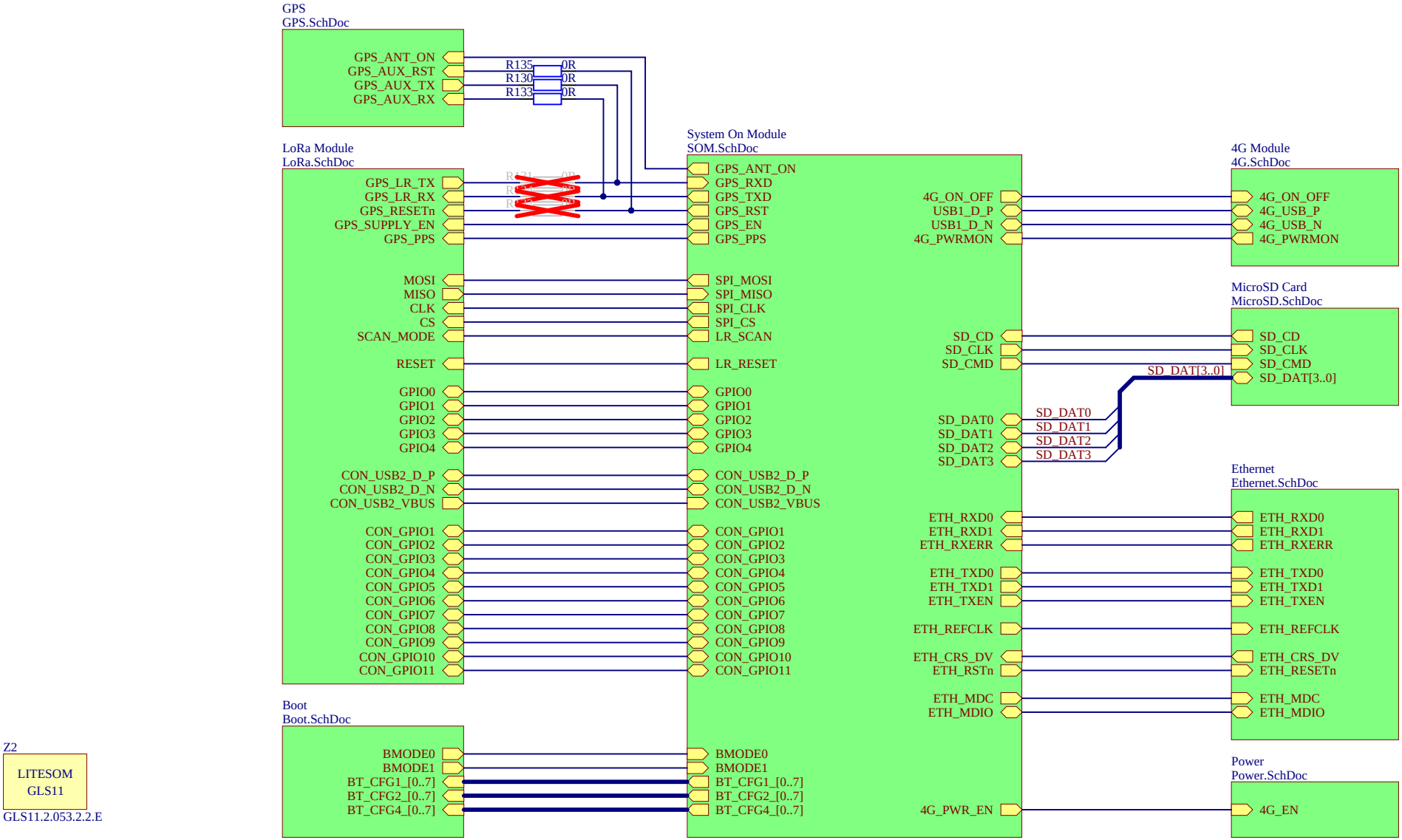


Z2
LITESOM
GLS11
GLS11.2.053.2.2.E

Z1
ENCLOSURE
HQ027S

Z11
PCB
Lora Gateway 1.3

MH3 MH4 MH1 MH2
GND GND GND GND

Z3 Z4 Z6 Z5
9771100360 9771100369 9771100360 9771100360
GND GND GND GND

Z7 Z8 Z9 Z10
M3 M3 M3 M3

FD1 FD2 FD3 FD4
FIDUCIAL FIDUCIAL FIDUCIAL FIDUCIAL

| | | | |
|---|---|---|---|
| Title | Main | | |
| Size | A4 | Project LoRa Linux Gateway | Rev 1.3.0 |
| Date | 2018-03-20 | Number 1 | Sheet 1 / 9 |

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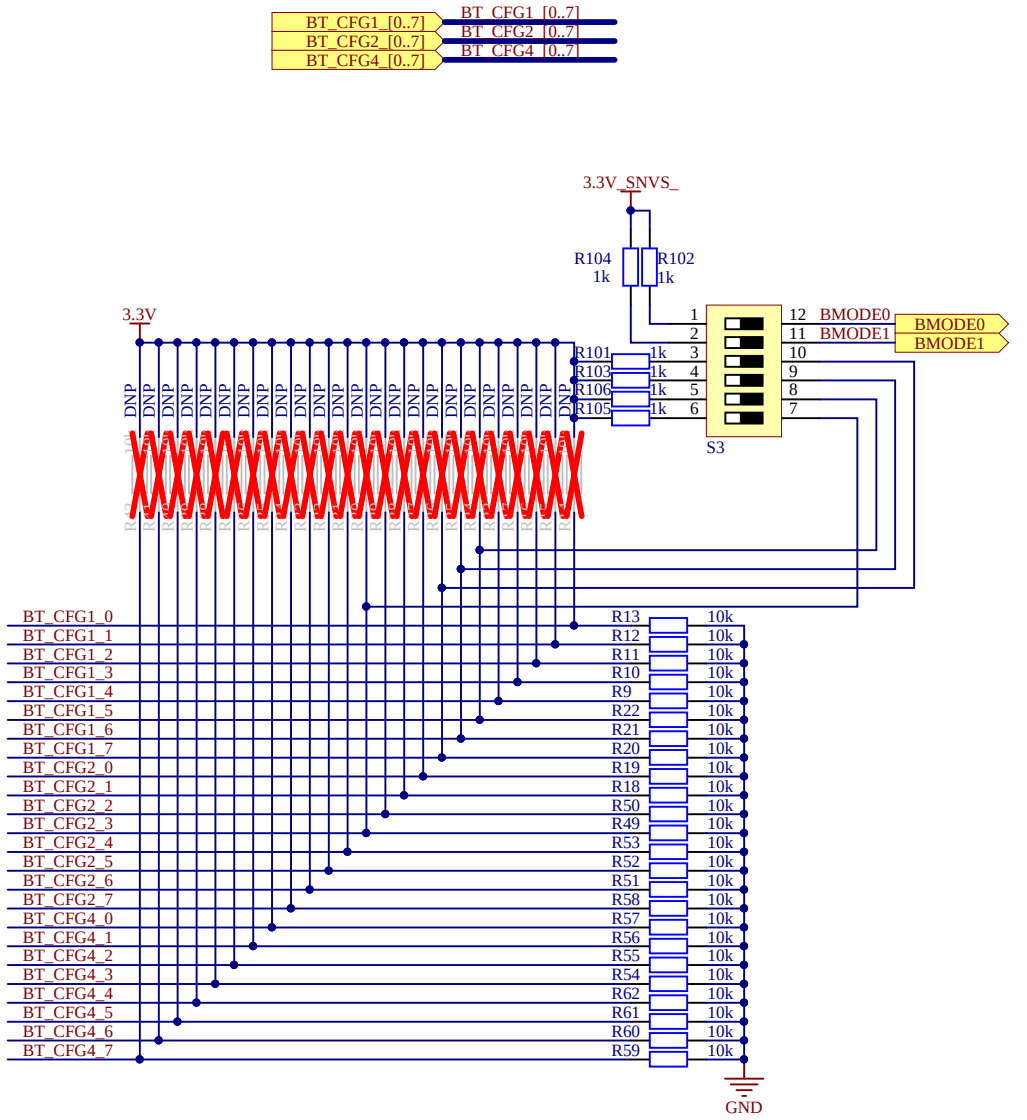
# FUSE MAP

<Default: QSPI BOOT>

| TYPE | BOOT_CFG1[7] | BOOT_CFG1[6] | BOOT_CFG1[5] | BOOT_CFG1[4] | BOOT_CFG1[3] | BOOT_CFG1[2] | BOOT_CFG1[1] | BOOT_CFG1[0] |
|---|---|---|---|---|---|---|---|---|
| | 0/1 | 0/1 | 0/1 | 1 | 0 | 0 | 0 | 0 |
| QSPI | 0 | 0 | 0 | 1 | Reserved | DDRSMP: "000" : Default "001-111" | | |
| WEIM | 0 | 0 | 0 | 0 | Memory Type: 0 - NOR Flash 1 - OneNAND | Reserved | Reserved | Reserved |
| Serial-ROM | 0 | 0 | 1 | 1 | Reserved | Reserved | Reserved | Reserved |
| SD/eSD | 0 | 1 | 0 | Fast Boot: 0 - Regular 1 - Fast Boot | SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104 | | SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only) | SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct |
| MMC/eMMC | 0 | 1 | 1 | Fast Boot: 0 - Regular 1 - Fast Boot | SD/MMC Speed 0 - Highl 1- Normal | Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled | SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only) | SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct |
| NAND | 1 | BT_TOGGLEMODE | Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256 | | Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved | | Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5 | |

| TYPE | BOOT_CFG2[7] | BOOT_CFG2[6] | BOOT_CFG2[5] | BOOT_CFG2[4] | BOOT_CFG2[3] | BOOT_CFG2[2] | BOOT_CFG2[1] | BOOT_CFG2[0] |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| QSPI | Reserved | HSPH0: Half Speed Phase Selection '0': select sampling at non-inverted clock '1': select sampling at inverted clock | HSDLY: Half Speed Delay selection '0': one clock delay '1': two clock delay | FSPH0: Full Speed Phase Selection '0': select sampling at non-inverted clock '1': select sampling at inverted clock | FSDLY: Full Speed Delay selection '0': one clock delay '1': two clock delay | Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz | Reserved | Reserved |
| WEIM | Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11- Reserved | | OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved | | Reserved | Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz | Reserved | Reserved |
| Serial-ROM | Reserved | Reserved | Reserved | Reserved | Reserved | Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz | Reserved | Reserved |
| SD/eSD | SD Calibration Step '00' - 1 TBD | | Bus Width: 0 - 1-bit 1 - 4-bit | | Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved | Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz | SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V | Reserved |
| MMC/eMMC | Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved. | | | | Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved | Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz | SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V | Reserved |
| NAND | Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. | | | | BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8 | Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz | Reset Time '0' - 12ms '1' - 22ms (LBA Nand) | Reserved |

| TYPE | BOOT_CFG4[7] | BOOT_CFG4[6] | BOOT_CFG4[5] | BOOT_CFG4[4] | BOOT_CFG4[3] | BOOT_CFG4[2] | BOOT_CFG4[1] | BOOT_CFG4[0] |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x450 | Infinit-Loop (Debug USE only) 0 - Disable 1- Enable | EEPROM Recovery Enable '0' - Disabled '1' - Enabled | CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3 | | SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit) | | Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved | |
| 0x460 | L2_HW_INVALIDATE_DISABLE | Reserved | FORCE_COLD_BOOT (Reflected in SBMR2) | BT_FUSE_SEL | DIR_BT_DIS | Reserved | SEC_CONFIG[1] | Reserved |
| 0x460 | Reserved (DDR3 config options) | | | | | | | |
| 0x460 | JTAG_SMODE[1:0] | WDOG_ENABLE '0' - Disabled '1' - Enabled | SJC_DISABLE | Reserved | Reserved | Reserved | Reserved | Reserved |
| 0x460 | Reserved | Reserved | Reserved | TZASC_ENABLE | JTAG_HEO | KTE | Reserved | DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/Emmc |




| BMODE[1:0] | BOOT TYPE |
|---|---|
| 00 | Boot From Fuses |
| 01 | Serial Downloader |
| 10 | Internal Boot (Development) |
| 11 | Reserved |

| | | | |
|---|---|---|---|
| Title | Booting Resistors | | |
| Size | A4 | Project LoRa Linux Gateway | Rev 1.3.0 |
| Date | 2018-03-20 | Number 2 | Sheet 2 / 9 |

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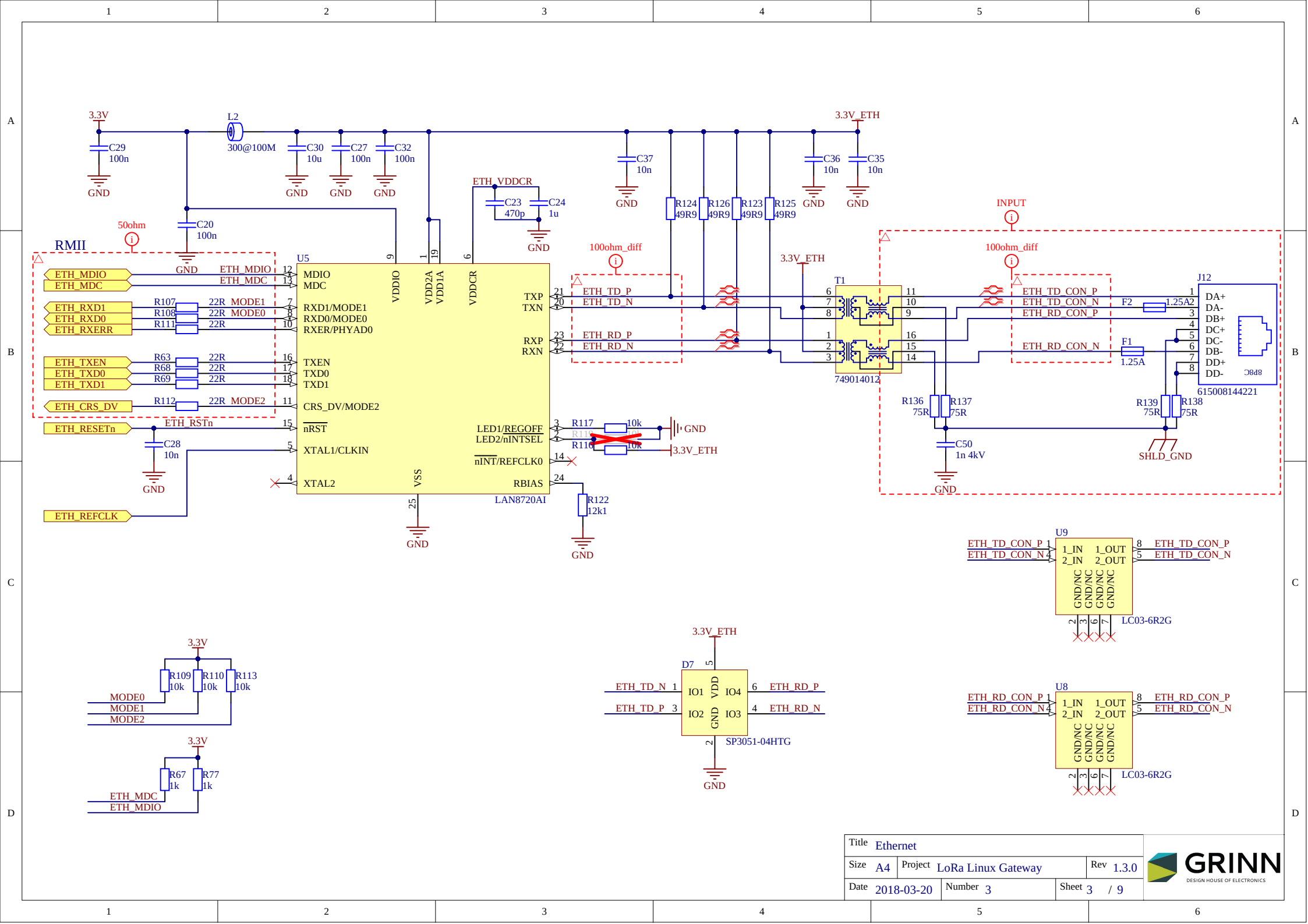


| | | | |
|---|---|---|---|
| Title | Ethernet | | |
| Size | A4 | Project LoRa Linux Gateway | Rev 1.3.0 |
| Date | 2018-03-20 | Number 3 | Sheet 3 / 9 |

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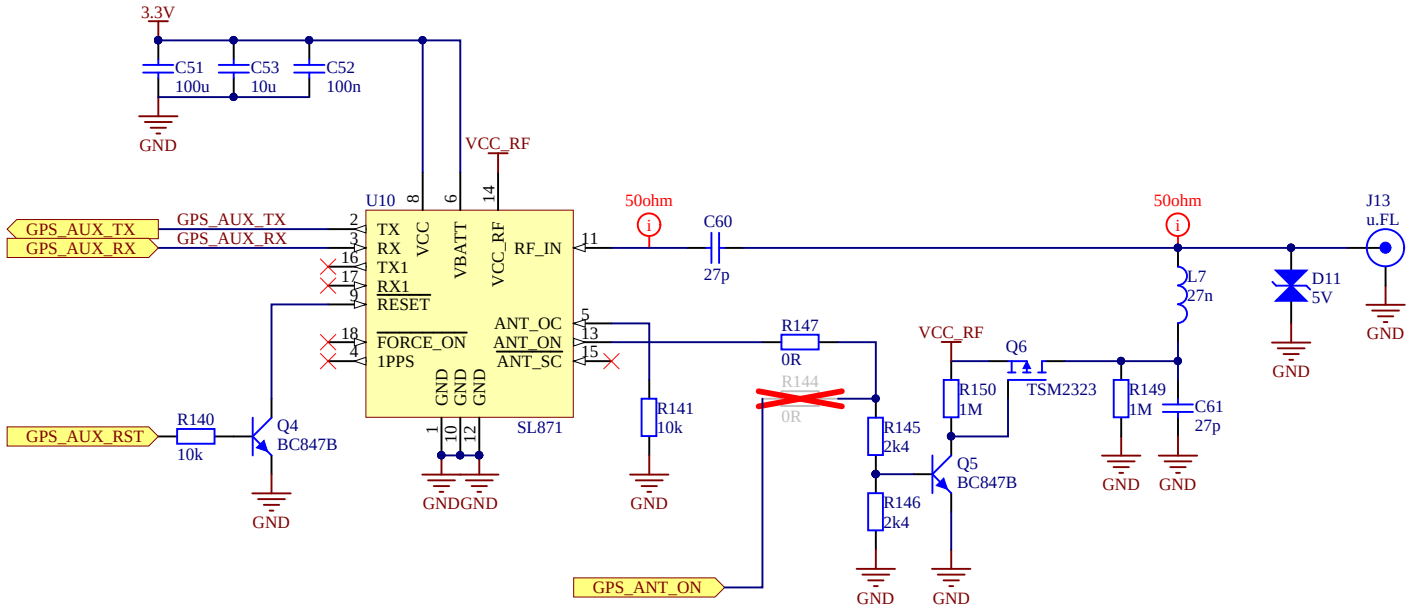
Murata LQG15HS27NJ02 Inductor - 0.65 dB of additional signal loss
Quarter wave stub on FR4 - 0.59 dB of additional signal loss
Coilcraft B09TJLC Inductor (used in ref. design) - 0.37 dB of additional signal loss




*ANT_ON is for the first gen of receiver

| | | | |
|---|---|---|---|
| Title | GPS module | | |
| Size | A4 | Project LoRa Linux Gateway | Rev 1.3.0 |
| Date | 2018-03-20 | Number 4 | Sheet 4 / 9 |

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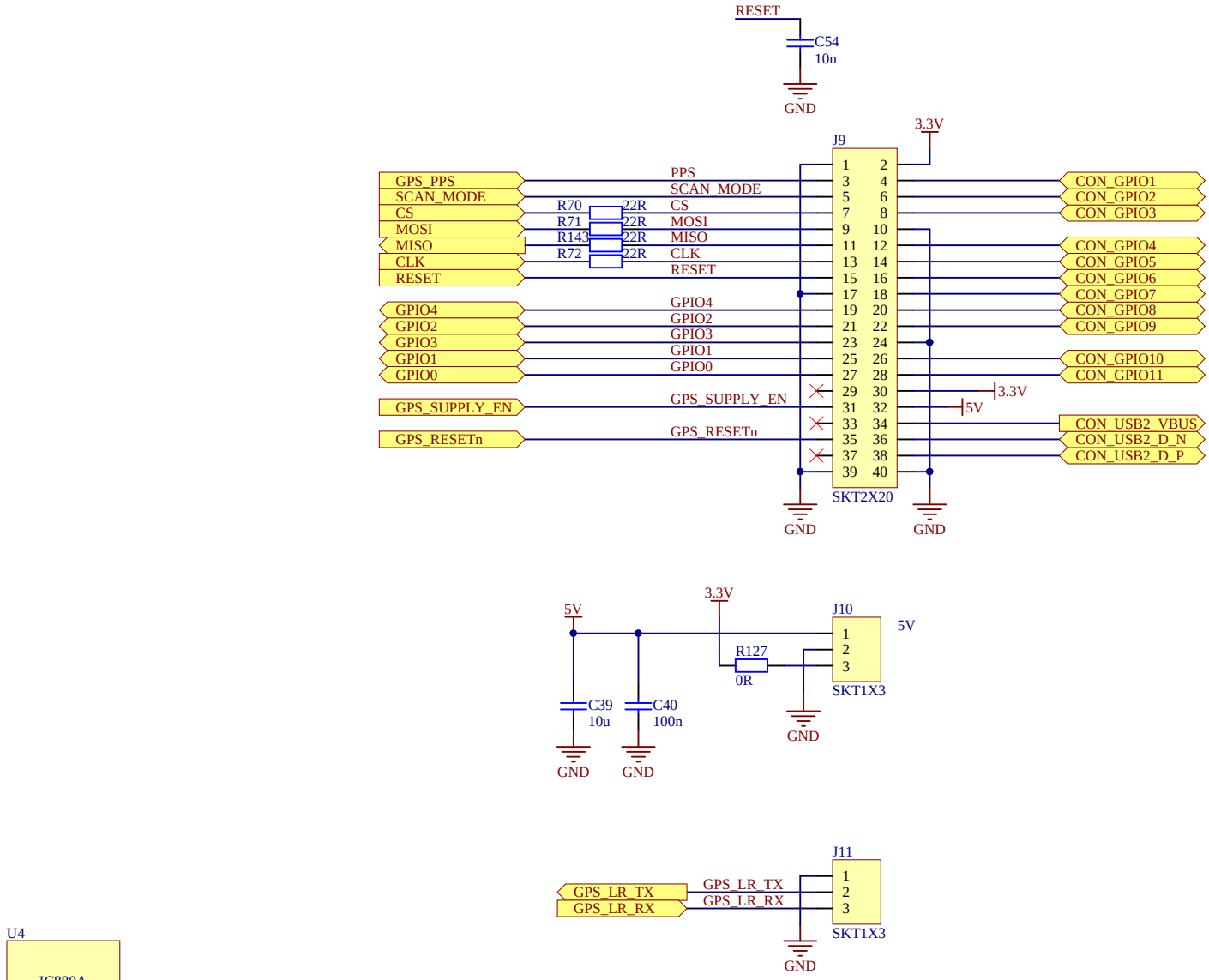


| | | | |
|---|---|---|---|
| Title | LoRa Module | | |
| Size | A4 | Project LoRa Linux Gateway | Rev 1.3.0 |
| Date | 2018-03-20 | Number 5 | Sheet 5 / 9 |

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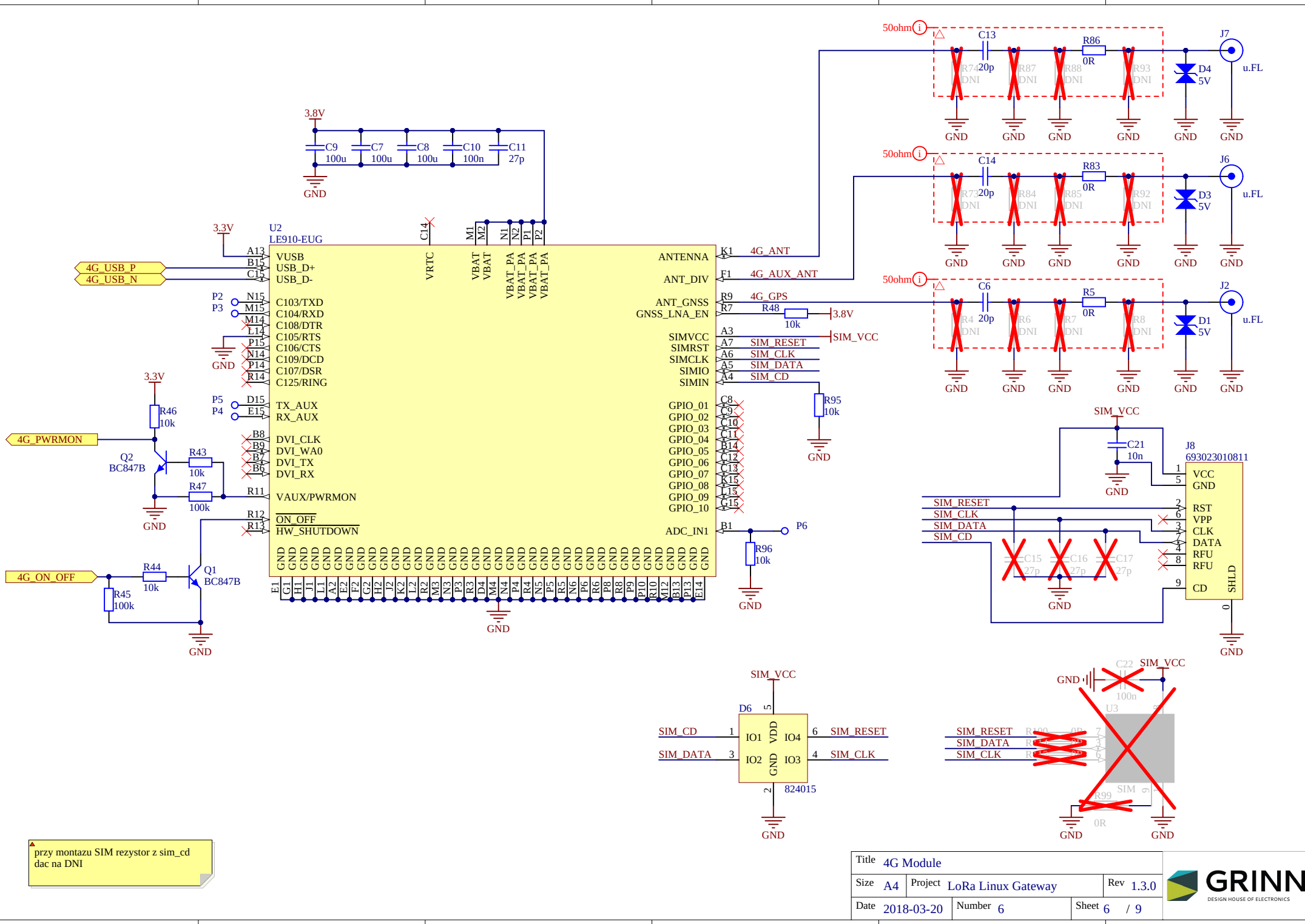
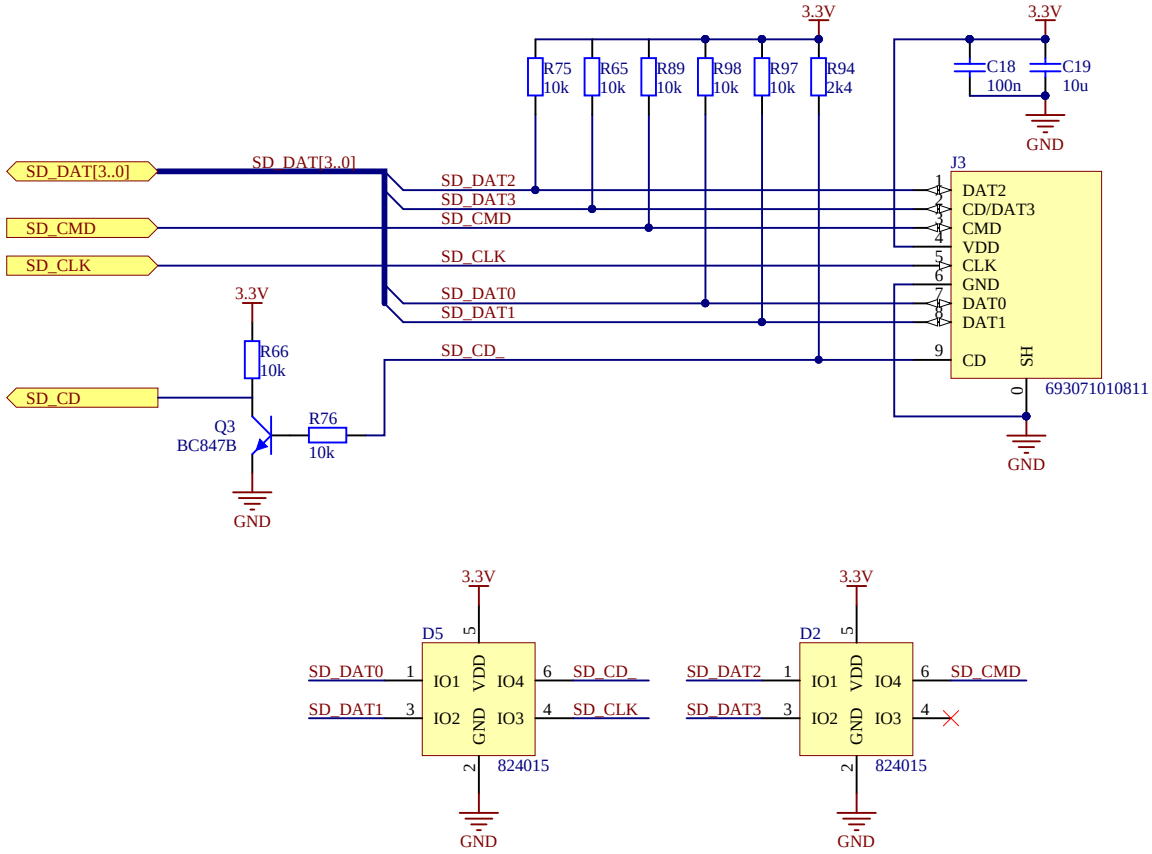
DESIGN HOUSE OF ELECTRONICS


U2
LE910-EUG
3.8V
3.3V
GND
4G_USB_P
4G_USB_N
4G_PWRMON
4G_ON_OFF
4G_ANT
4G_AUX_ANT
4G_GPS
SIM_VCC
SIM_RESET
SIM_CLK
SIM_DATA
SIM_CD
50ohm
u.FL
J7
J6
J2
J8
693023010811
P6
D6
824015
U3
przy montazu SIM rezystor z sim_cd dac na DNI
Title 4G Module
Size A4
Project LoRa Linux Gateway
Rev 1.3.0
Date 2018-03-20
Number 6
Sheet 6 / 9
GRINN
DESIGN HOUSE OF ELECTRONICS




| | | | |
|---|---|---|---|
| Title | Micro SD Card Socket | | |
| Size | A4 | Project LoRa Linux Gateway | Rev 1.3.0 |
| Date | 2018-03-20 | Number 7 | Sheet 7 / 9 |

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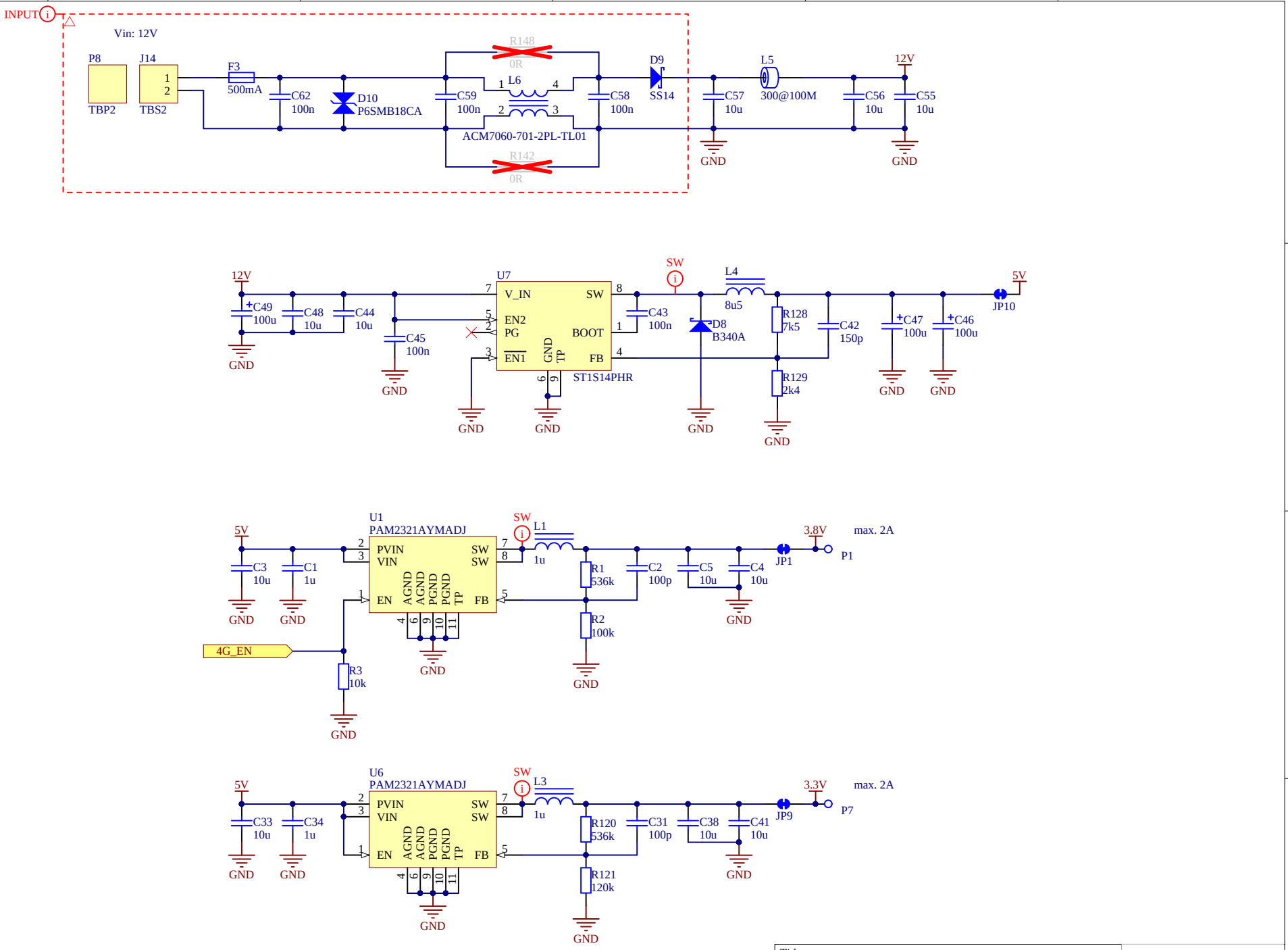
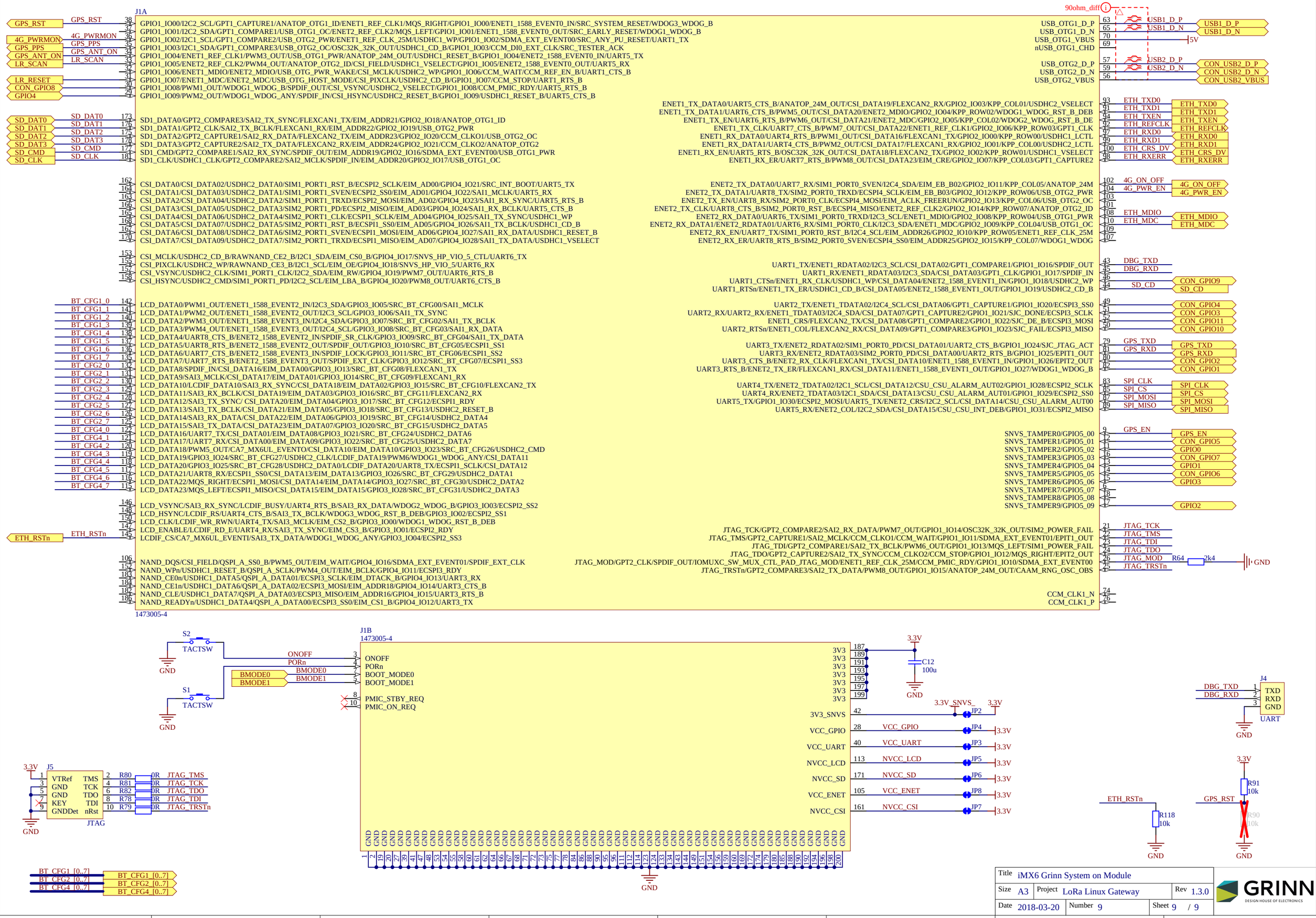
DESIGN HOUSE OF ELECTRONICS




| | | | |
|---|---|---|---|
| Title | Power | | |
| Size | A4 | Project LoRa Linux Gateway | Rev 1.3.0 |
| Date | 2018-03-20 | Number 8 | Sheet 8 / 9 |

GRINN
DESIGN HOUSE OF ELECTRONICS




| | |
|---|---|
| Title | iMX6 Grinn System on Module |
| Size | A3 |
| Project | LoRa Linux Gateway |
| Rev | 1.3.0 |
| Date | 2018-03-20 |
| Number | 9 |
| Sheet | 9 / 9 |

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