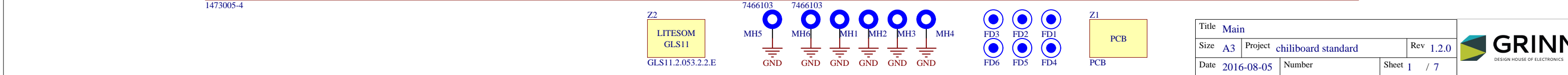
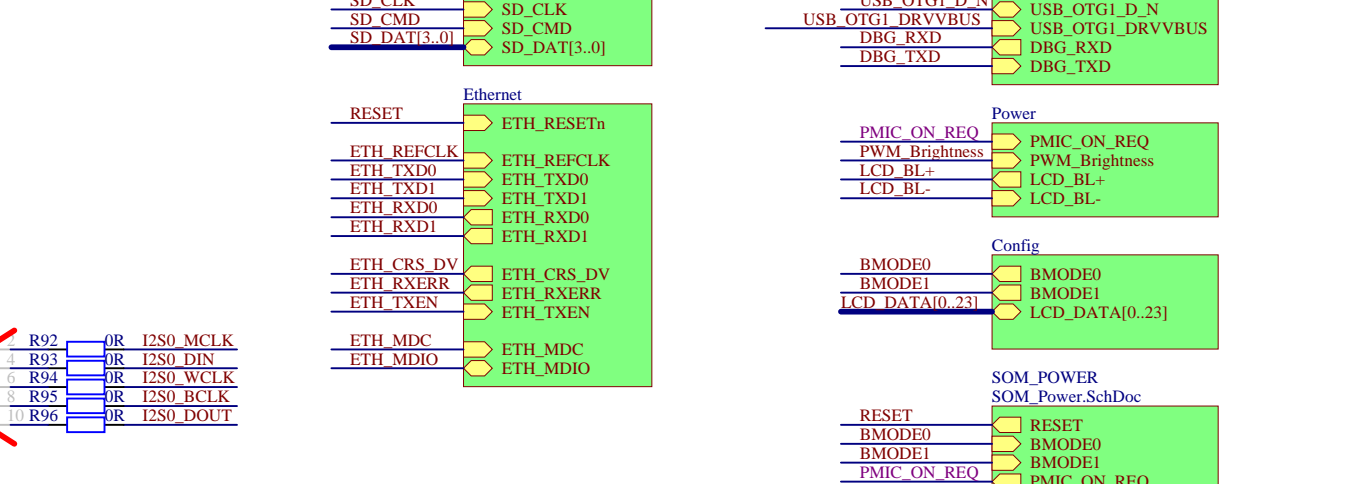
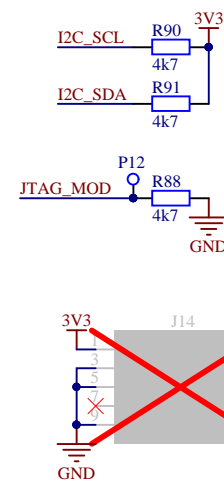
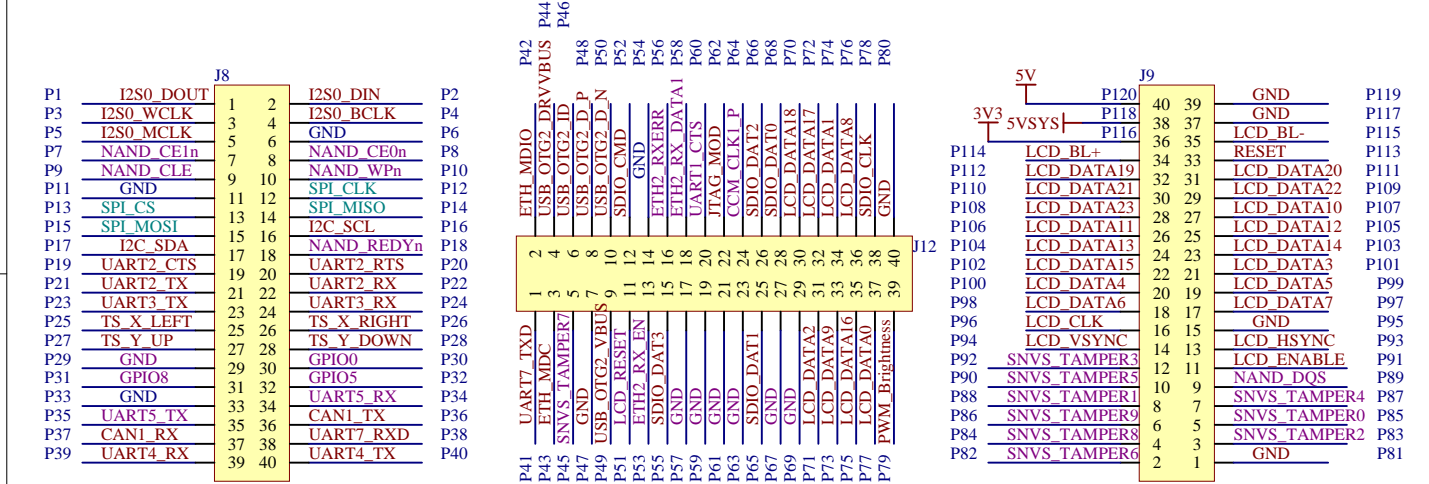
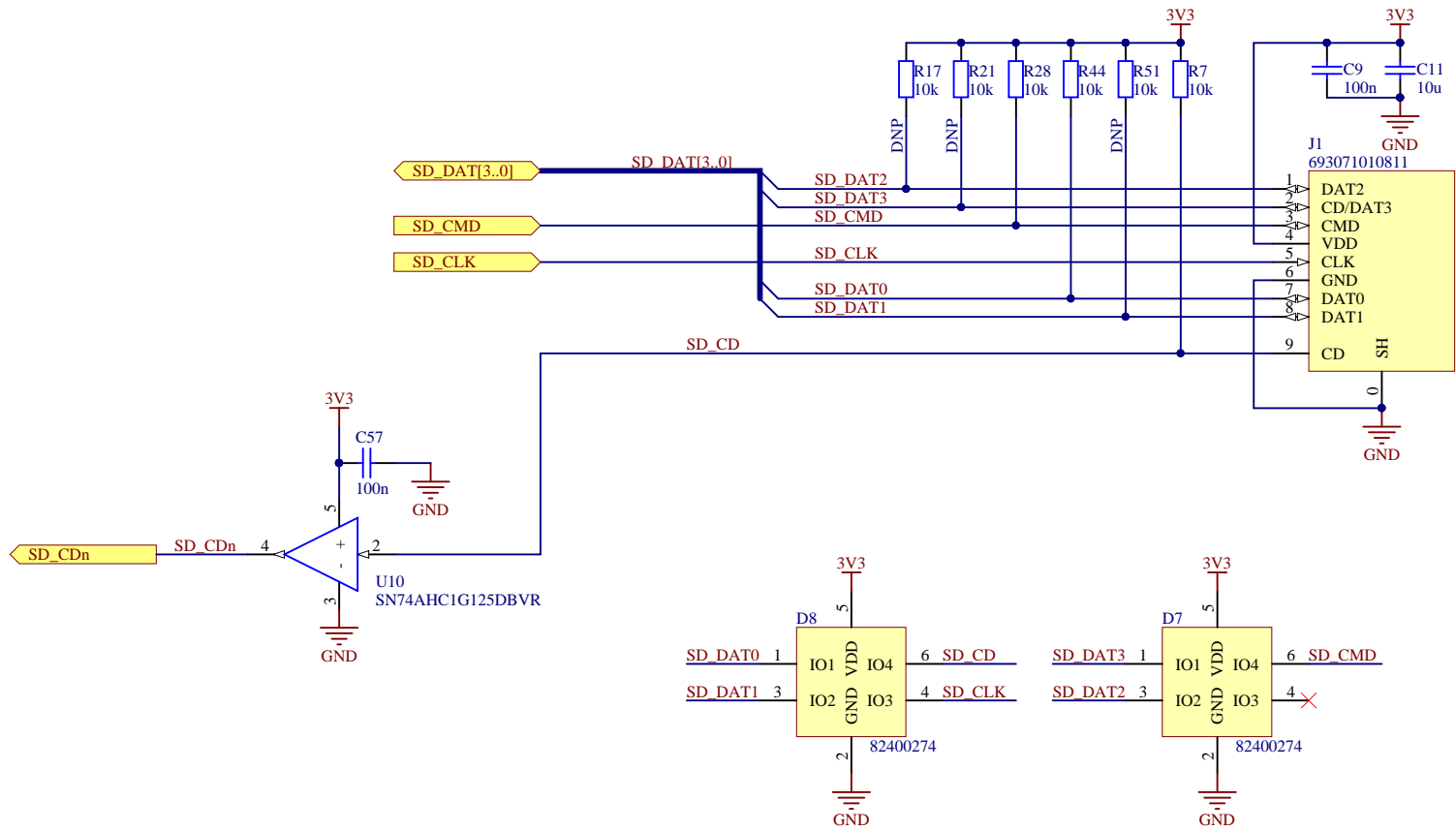


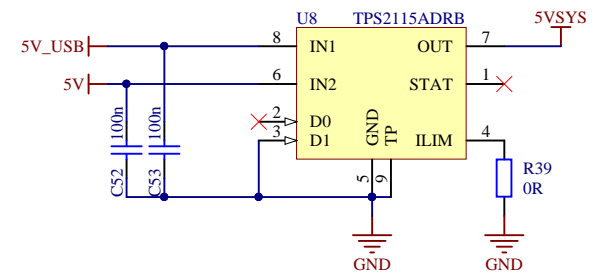
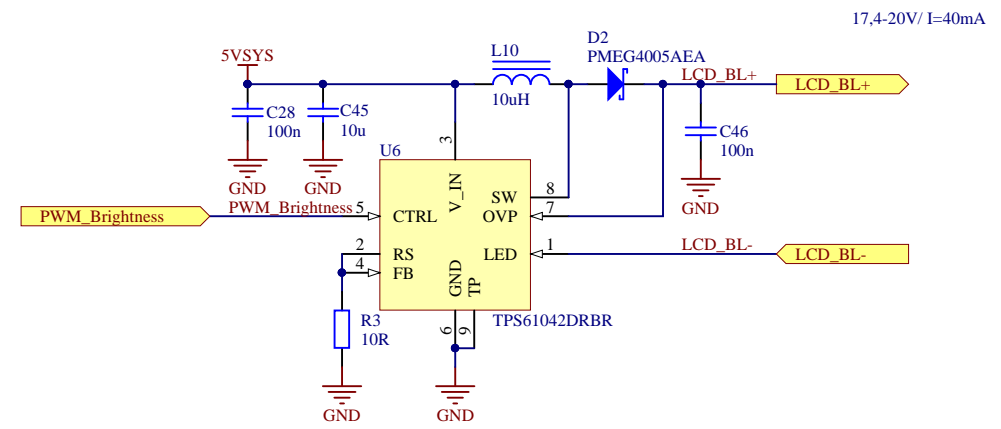
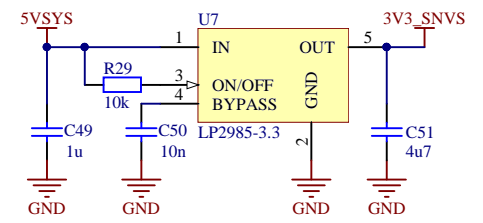
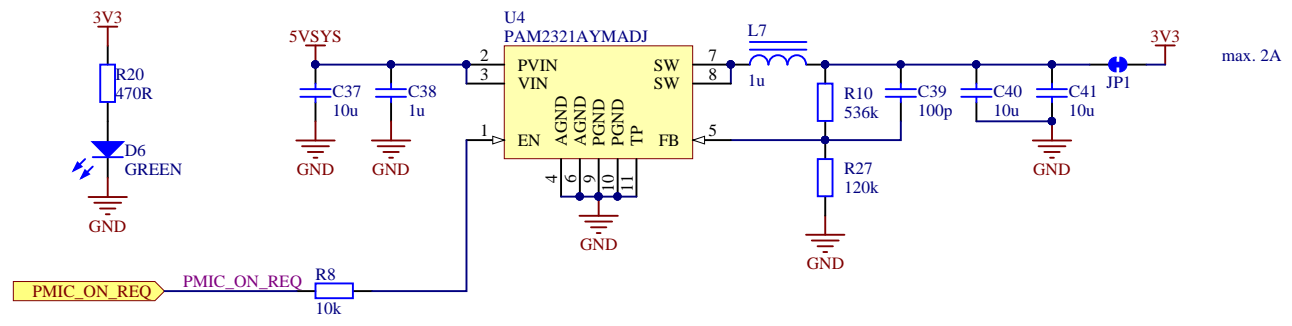
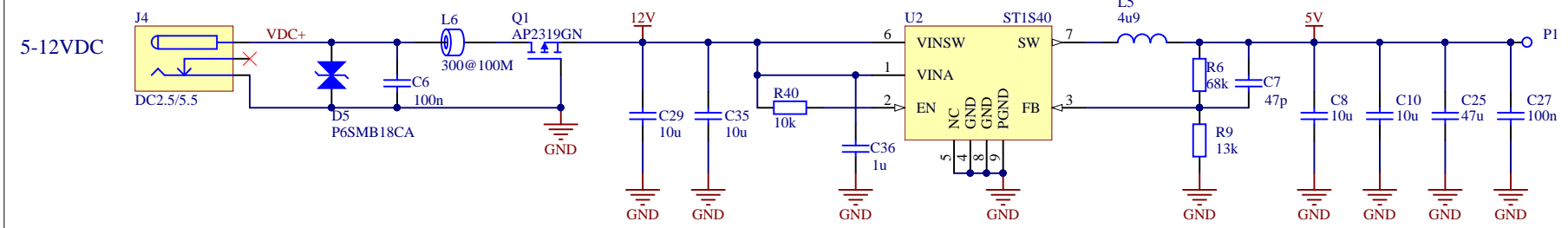
ChiliBoard Sandwich Connectors





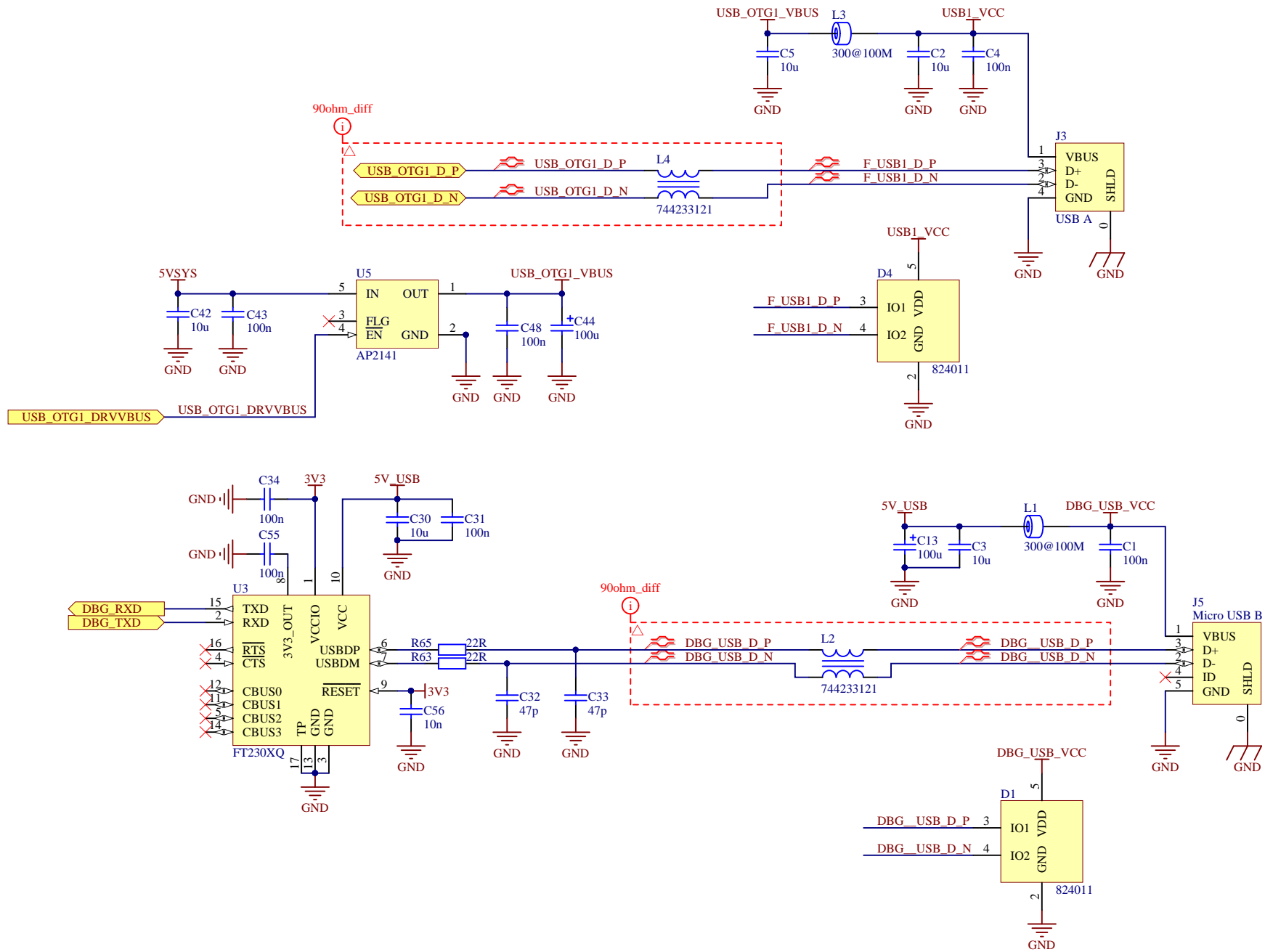
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|-------|------------|----------------------|---------------------|
| Title | | Micro SD Card Socket | |
| Size | A4 | Project | chiliboard standard |
| Date | 2016-08-05 | Rev | 1.2.0 |
| | | Number | |
| | | Sheet | 3 / 7 |





| | | | |
|-------|------------|--------------|---------------------|
| Title | | Power Supply | |
| Size | A4 | Project | chiliboard standard |
| Date | 2016-08-05 | Rev | 1.2.0 |
| | | Number | * |
| | | Sheet | 4 / 7 |





| | | | |
|-----------------|-----------------------------|-------------|--|
| Title USB | | | |
| Size A4 | Project chiliboard standard | Rev 1.2.0 | |
| Date 2016-08-05 | Number * | Sheet 5 / 7 | |



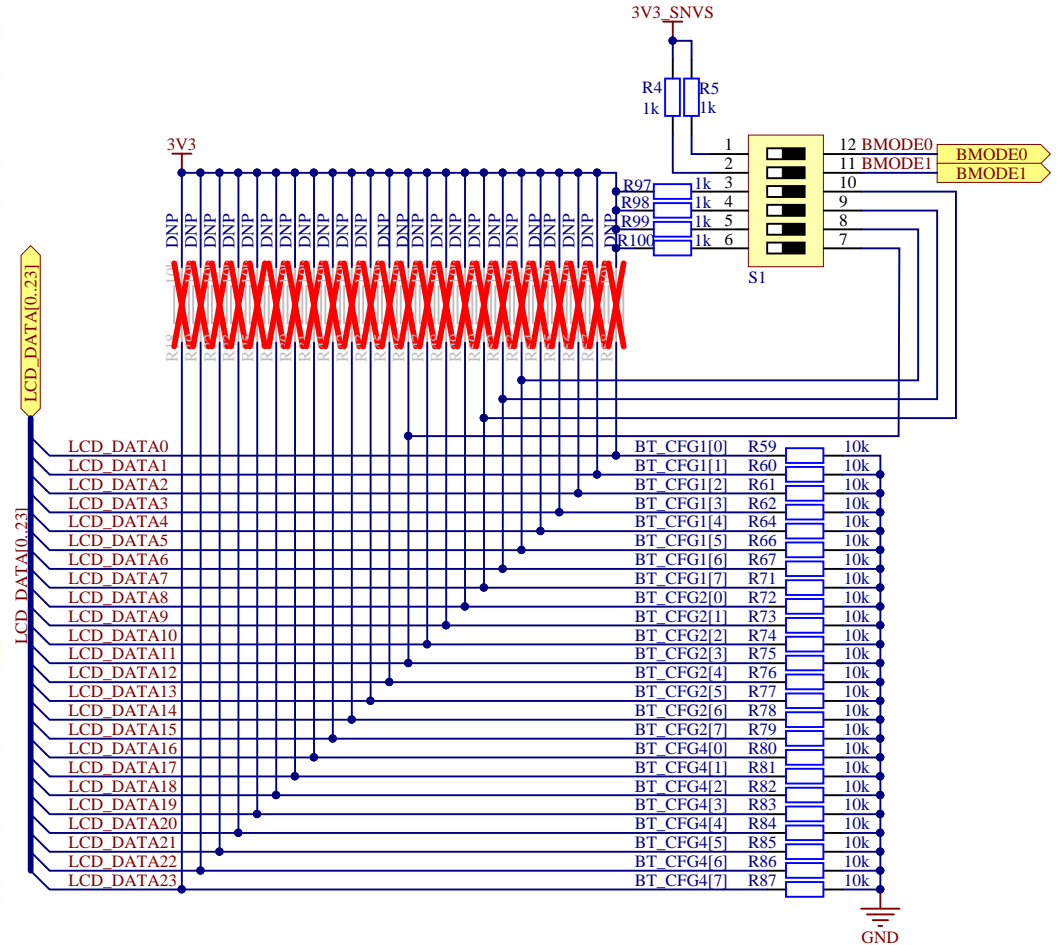
FUSE MAP

<Default: QSPI BOOT>

| TYPE | BOOT_CFG1[7] | BOOT_CFG1[6] | BOOT_CFG1[5] | BOOT_CFG1[4] | BOOT_CFG1[3] | BOOT_CFG1[2] | BOOT_CFG1[1] | BOOT_CFG1[0] |
|------------|--------------|---------------|---|--|--|--|--|---|
| QSPI | 0 | 0 | 0 | 1 | Reserved | | | |
| WEIM | 0 | 0 | 0 | 0 | Memory Type: 0 - NOR Flash 1 - OneNAND | Reserved | Reserved | Reserved |
| Serial-ROM | 0 | 0 | 1 | 1 | Reserved | Reserved | Reserved | Reserved |
| SD/eSD | 0 | 1 | 0 | Fast Boot: 0 - Regular 1 - Fast Boot | SD/GPIO Speed 00 - Normal/SDR12 01 - High/SDR23 10 - SDR50 11 - SDR104 | SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDMC_RST pad (USDMC2 & 4 only) | SD Loopback Clock Source 0 - Serial-SD pad and SDR104 only 1 - through SD pad 2 - direct | |
| MMC/eMMC | 0 | 1 | 1 | Fast Boot: 0 - Regular 1 - Fast Boot | SD/MMC Speed 0 - High 1 - Normal | Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled | SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDMC_RST pad (USDMC2 & 4 only) | SD Loopback Clock Source 0 - Serial-SD pad and SDR104 only 1 - through SD pad 2 - direct |
| NAND | 1 | BT_TOGGLEMODE | Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256 | | Nand Number of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved | | Nand Row address bytes: 00 - 3 01 - 2 10 - 4 11 - 5 | |

| TYPE | BOOT_CFG2[7] | BOOT_CFG2[6] | BOOT_CFG2[5] | BOOT_CFG2[4] | BOOT_CFG2[3] | BOOT_CFG2[2] | BOOT_CFG2[1] | BOOT_CFG2[0] |
|------------|--|---|--|---|--|--|---|--------------|
| QSPI | Reserved | HSPI: Half Speed Phase Selection 0 - Phase sampling at intermediate clock 1 - Phase sampling at maximum clock | HSPI: Half Speed Delay Selection 0 - One clock delay 1 - Two clock delay | HSPI: Full Speed Phase Selection 0 - Phase sampling at intermediate clock 1 - Phase sampling at maximum clock | HSPI: Full Speed Delay Selection 0 - One clock delay 1 - Two clock delay | Boot Frequencies (ARM/D2R) 00 - 500 / 400 MHz 01 - 250 / 200 MHz | Reserved | Reserved |
| WEIM | Musing Scheme: 00 - A/D16 01 - A/D8 10 - A/D4 11 - Reserved | | OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved | Reserved | Reserved | Boot Frequencies (ARM/D2R) 00 - 500 / 400 MHz 01 - 250 / 200 MHz | Reserved | Reserved |
| Serial-ROM | Reserved | Reserved | Reserved | Reserved | Reserved | Boot Frequencies (ARM/D2R) 00 - 500 / 400 MHz 01 - 250 / 200 MHz | Reserved | Reserved |
| SD/eSD | SD Calibration Step 00 - 1 TBD | Bus Width: 0 - 1-bit 1 - 4-bit | Reserved | Reserved | Reserved | Boot Frequencies (ARM/D2R) 00 - 500 / 400 MHz 01 - 250 / 200 MHz | SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V | Reserved |
| MMC/eMMC | Blue Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 011 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Etc - reserved | | Reserved | Reserved | Reserved | Boot Frequencies (ARM/D2R) 00 - 500 / 400 MHz 01 - 250 / 200 MHz | SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V | Reserved |
| NAND | Toggle Mode 33MHz Preamble Delay, Read Latency: 000 - 16 SPI/CCLK cycles 001 - 1 SPI/CCLK cycles 010 - 2 SPI/CCLK cycles 011 - 3 SPI/CCLK cycles 100 - 4 SPI/CCLK cycles 101 - 5 SPI/CCLK cycles 110 - 6 SPI/CCLK cycles 111 - 7 SPI/CCLK cycles | | Reserved | Reserved | Reserved | Boot Frequencies (ARM/D2R) 00 - 500 / 400 MHz 01 - 250 / 200 MHz | Reset Time 0 - 120ms 1 - 220ms (4BA NAND) | Reserved |

| TYPE | BOOT_CFG4[7] | BOOT_CFG4[6] | BOOT_CFG4[5] | BOOT_CFG4[4] | BOOT_CFG4[3] | BOOT_CFG4[2] | BOOT_CFG4[1] | BOOT_CFG4[0] |
|-------|---|---|---|---|--------------|--------------|---|---|
| 0x450 | Infinite-Loop (Debug USE only) 0 - Disable 1 - Enable | EEPROM Recovery Enable 0 - Disabled 1 - Enabled | CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3 | SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit) | | | Flash Select: 000 - eCS#1 001 - eCS#2 010 - eCS#3 011 - eCS#4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved | |
| 0x460 | L2_HW_INVALIDATE_DISABLE | Reserved | FORCE_COLD_BOOT (Reflected in SBMR2) | BT_FUSE_SEL | DIR_BT_DIS | Reserved | SEC_CONFIG[1] | Reserved |
| 0x460 | Reserved (DDR3 config options) | | | | | | | |
| 0x460 | JTAG_SMODE[1:0] | WDG_ENABLE 0 - Disabled 1 - Enabled | SJC_DISABLE | Reserved | Reserved | Reserved | Reserved | Reserved |
| 0x460 | Reserved | Reserved | Reserved | TZASC_ENABLE | JTAG_HEO | KTE | Reserved | DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC |



| BMODE[1:0] | BOOT TYPE |
|------------|-----------------------------|
| 00 | Boot From Fuses |
| 01 | Serial Downloader |
| 10 | Internal Boot (Development) |
| 11 | Reserved |

