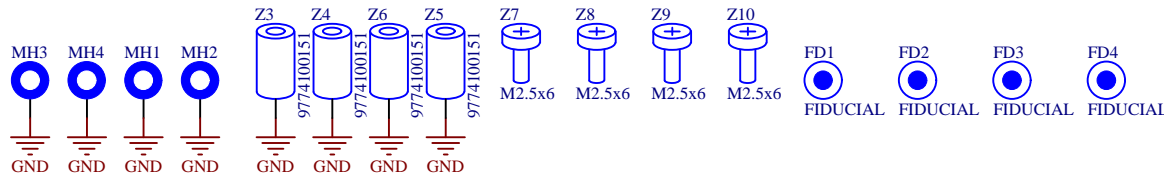


Z2
LITESOM
GLS11
GLS11.2.053.2.2.E

Z1
ENCLOSURE
HQ027S

PCB1
PCB
Lora Gateway 1.4



Title Main		Project LoRa Linux Gateway		Rev 1.4.0
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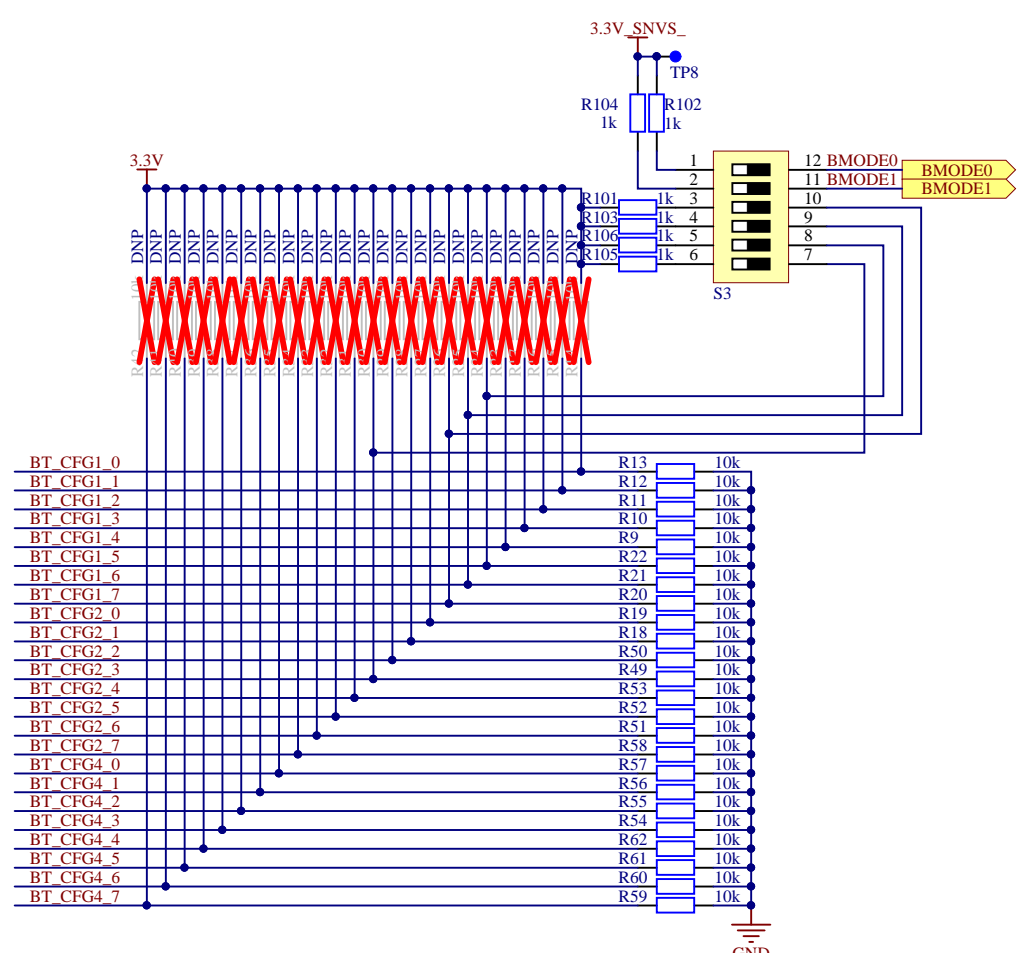
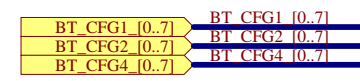


FUSE MAP <Default: QSPI BOOT>

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]	
QSPI	0	0	0	1	Reserved		DDRSMP: "000": Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved	
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved	
SD/eSD	0	1	0		Fast Boot: 0 - Regular 1 - Fast Boot	SD/eMMC Speed: 00 - Normal (SDR12) 01 - High (SDR25) 10 - SDR50 11 - SDR104	SD Power Cycle Enable: 0 - No power cycle 1 - Enabled via (SDHC_#PST pad) (uSDHC3 & 4 only)	SD Loopback Clock Source Selector (SDR10 and SDR104 only): 0 - through SD pad 1 - direct	
MMC/eMMC	0	1	1		Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed: 0 - High 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable: 0 - No power cycle 1 - Enabled via (SDHC_#PST pad) (uSDHC3 & 4 only)	SD Loopback Clock Source Selector (SDR10 and SDR104 only): 0 - through SD pad 1 - direct
NAND	1	BT_TOGGLEMODE			Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256	Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved	Nand, Row, address, bytes: 00 - 3 01 - 3 10 - 4 11 - 5		

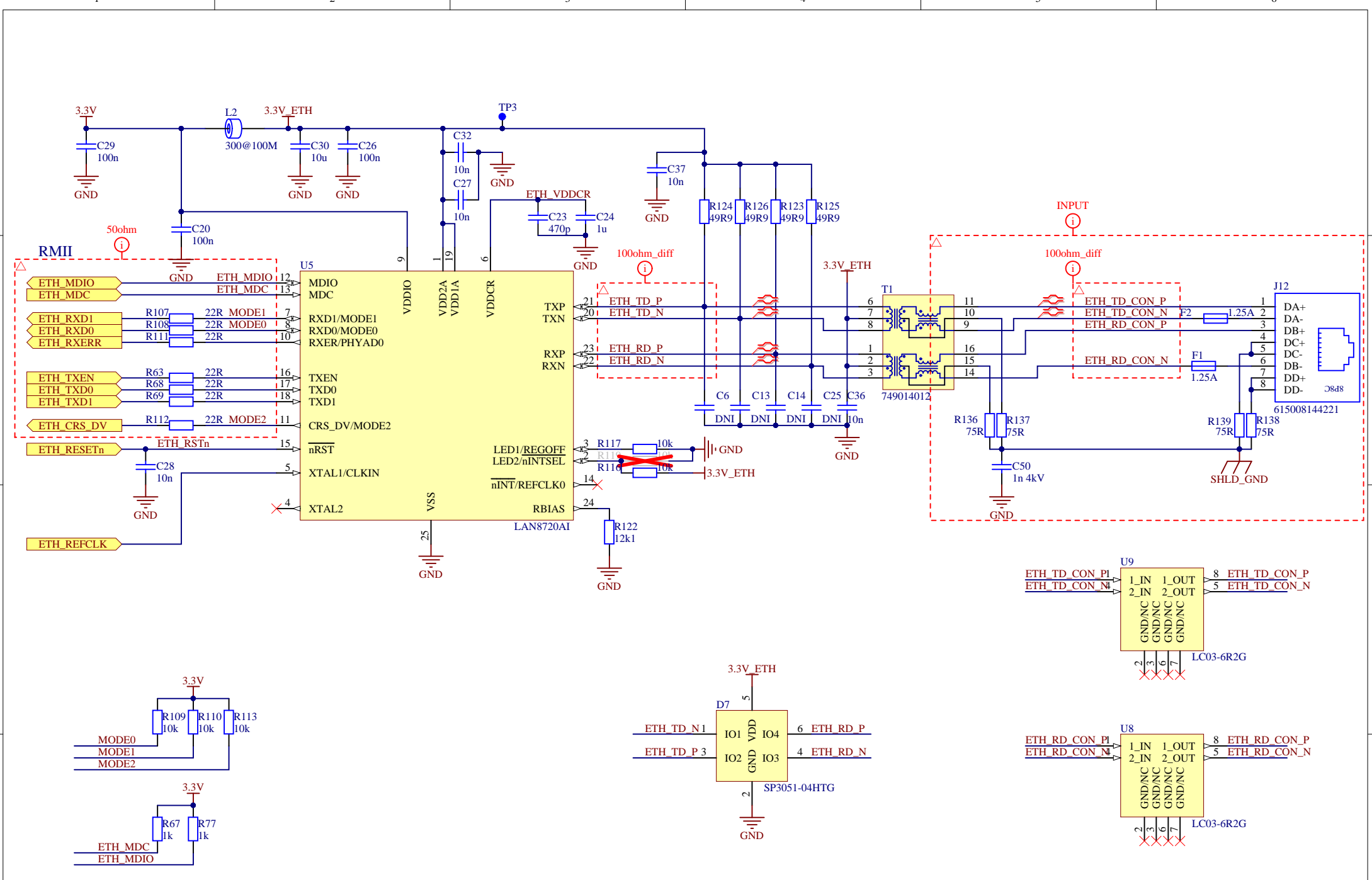
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved						Reserved	Reserved
WEIM	Moving Scheme: 00 - A#DIE 01 - A#DH 10 - A#DL 11 - Reserved				OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 '10' - TBD		Bus Width: 0 - 1-bit 1 - 4-bit		Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DDR): 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION: 0 - 3.0V 1 - 3.3V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 16-bit DDR (MMIO 4-8) 110 - 8-bit DDR (MMIO 4-8) 111 - Reserved				Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DDR): 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION: 0 - 3.0V 1 - 3.3V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: 000 - 16 @PMICLK cycles 001 - 1 @PMICLK cycles 010 - 2 @PMICLK cycles 011 - 3 @PMICLK cycles 100 - 4 @PMICLK cycles 101 - 5 @PMICLK cycles 110 - 6 @PMICLK cycles 111 - 7 @PMICLK cycles				BOOT_SBARCM_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8	Boot Frequency (ARM/DDR): 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Boot Time: 0 - 12ms 1 - 25ms (1.64 NAND)	Reserved

TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinite-Loop (Debug USE only) 0 - Disable 1 - Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3	SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)			Port Select: 000 - eCP12 001 - eCP18 010 - eCP18 011 - eCP18 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC

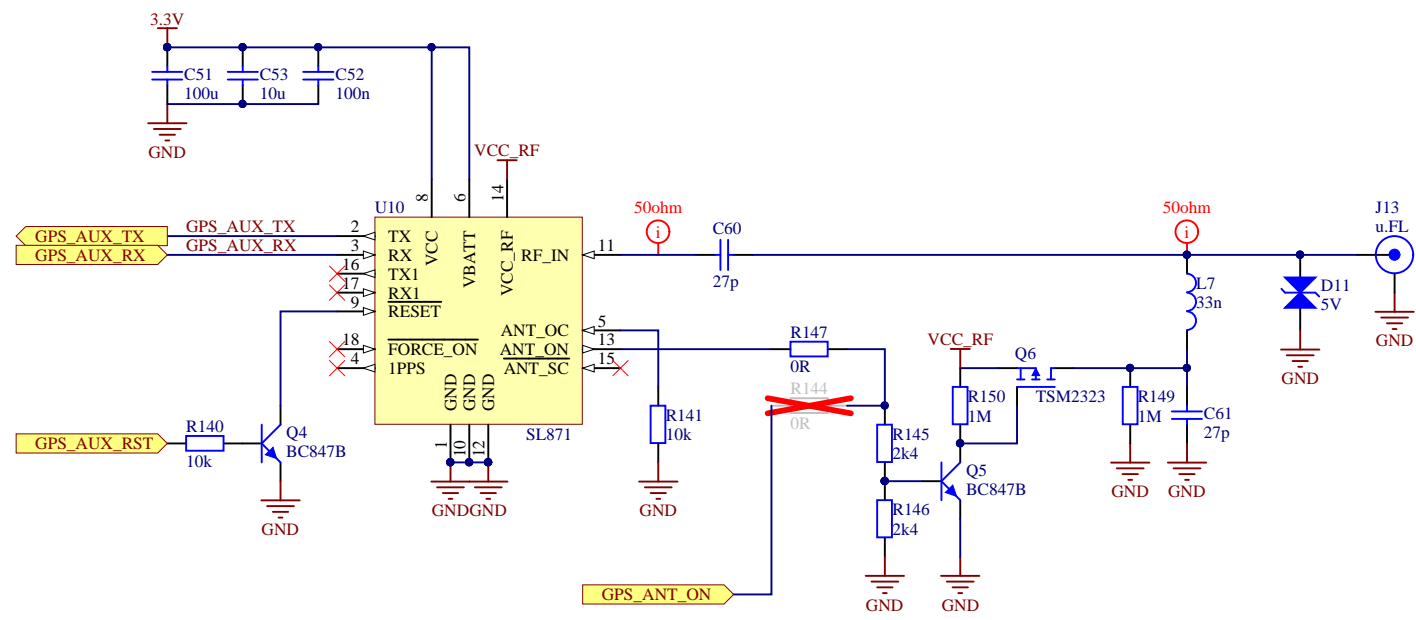


BMODE [1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

Title Booting Resistors
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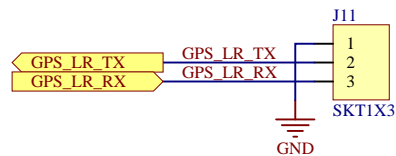
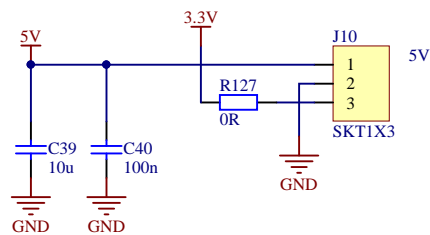
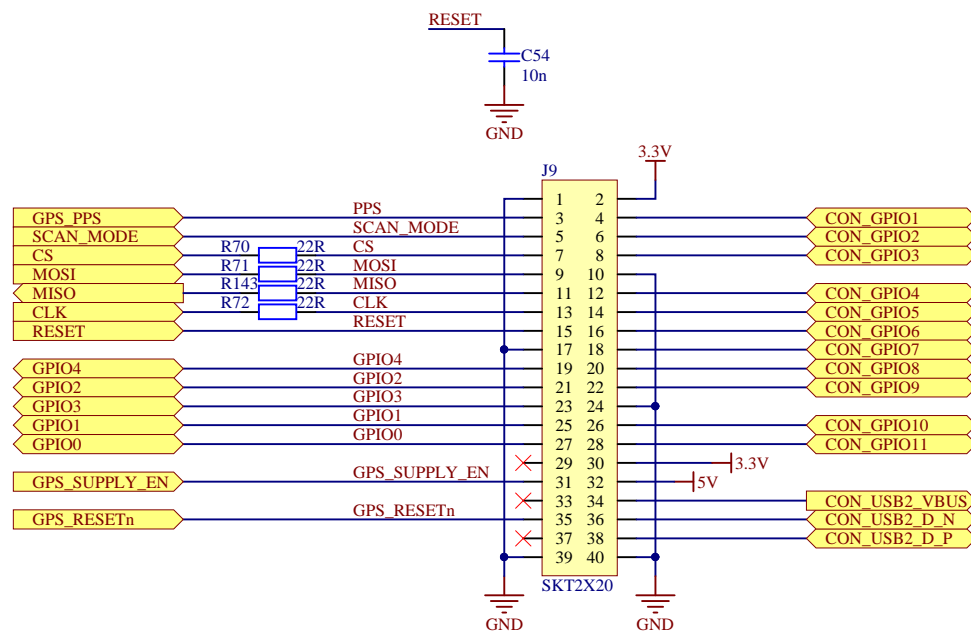
▲ Murata LQG15HS27NJ02 Inductor - 0.65 dB of additional signal loss
 Quarter wave stub on FR4 - 0.59 dB of additional signal loss
 Coilcraft B09TJLC Inductor (used in ref. design) - 0.37 dB of additional signal loss



*ANT_ON is for the first gen of receiver

Title		GPS module	
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U4
IC880A
WiMOD iC880A

Title		LoRa Module	
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A

B

C

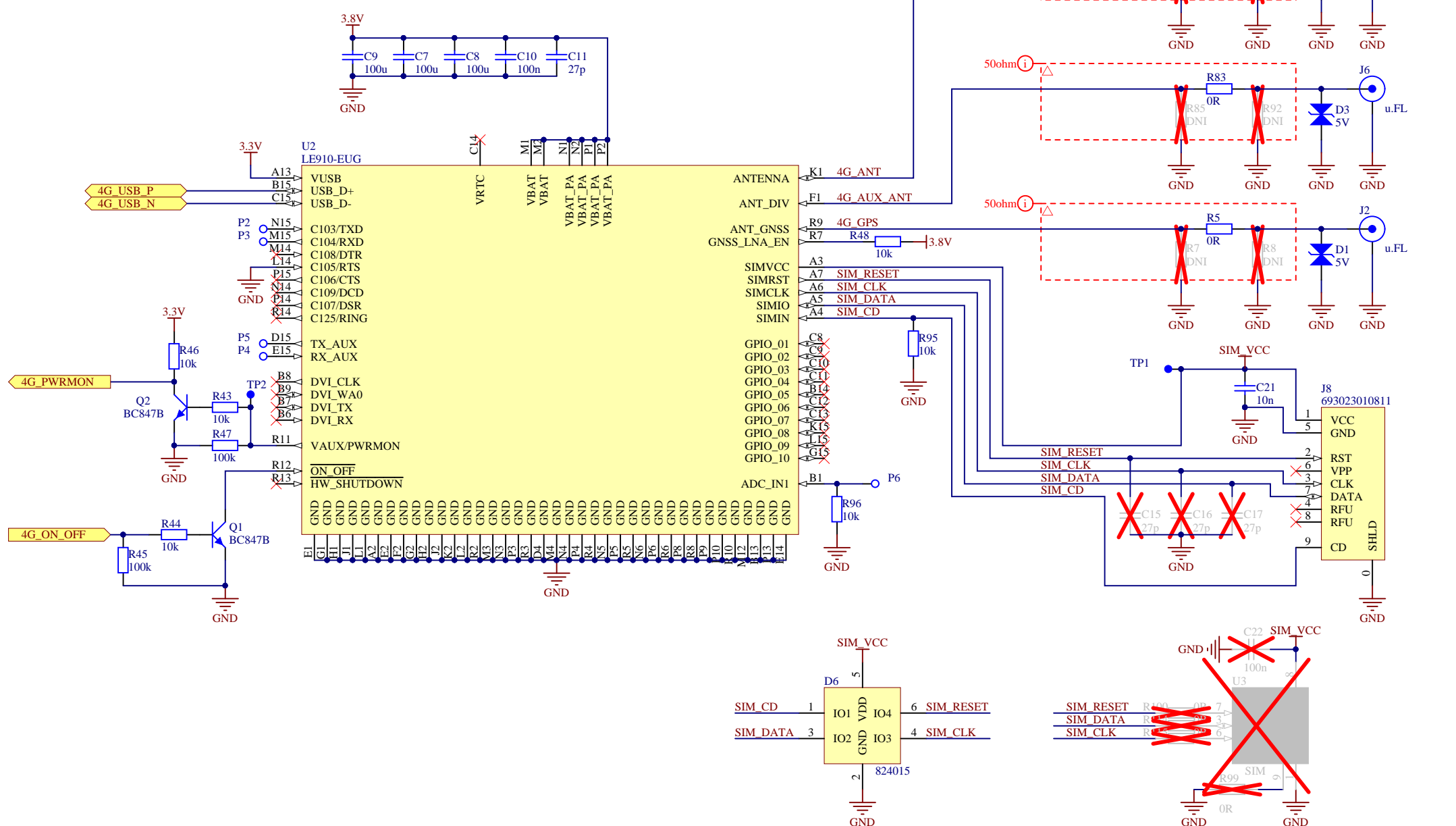
D

A

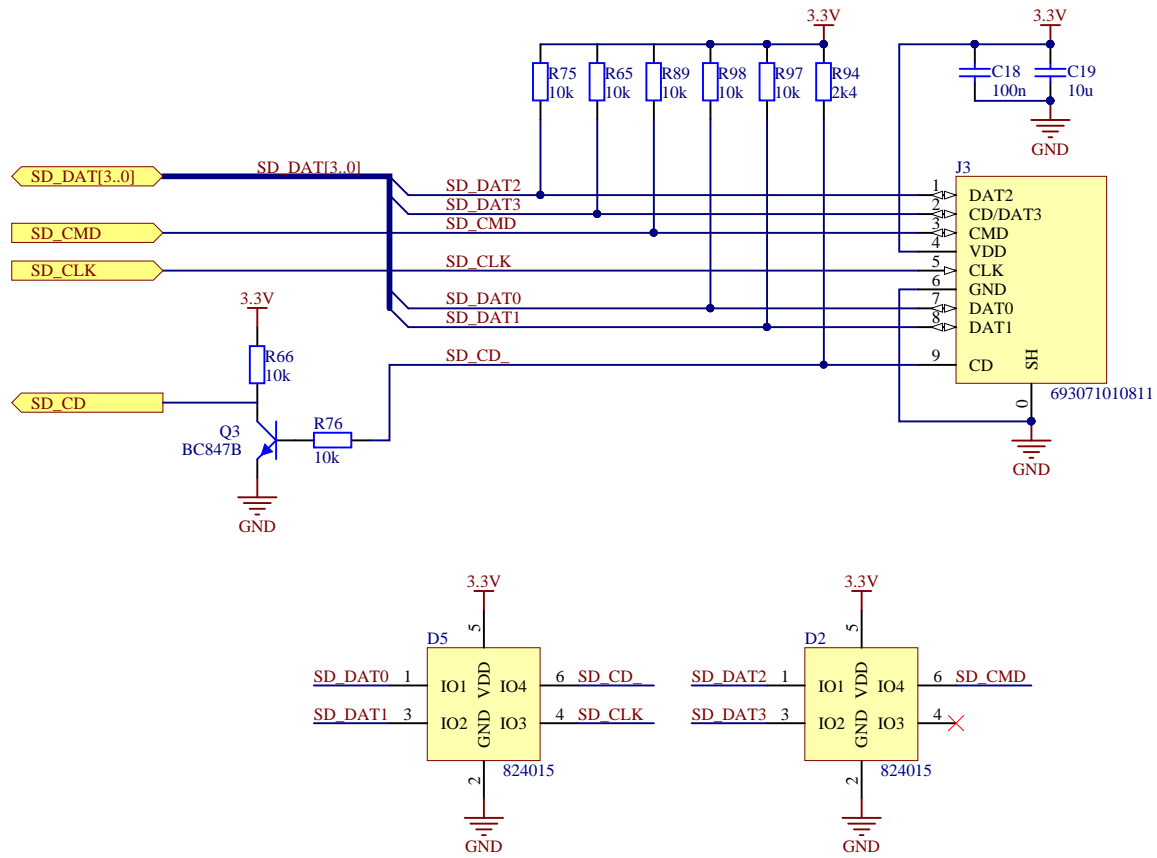
B

C

D

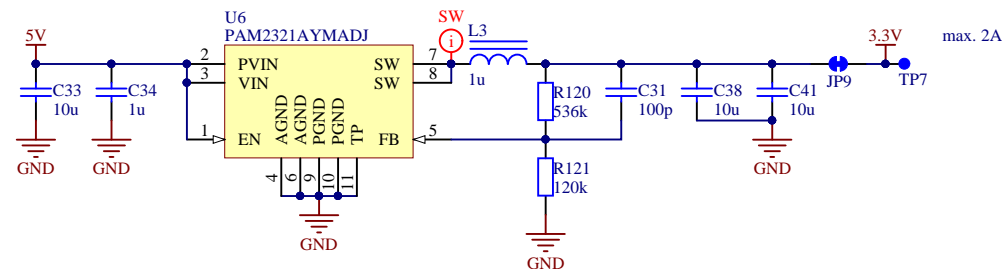
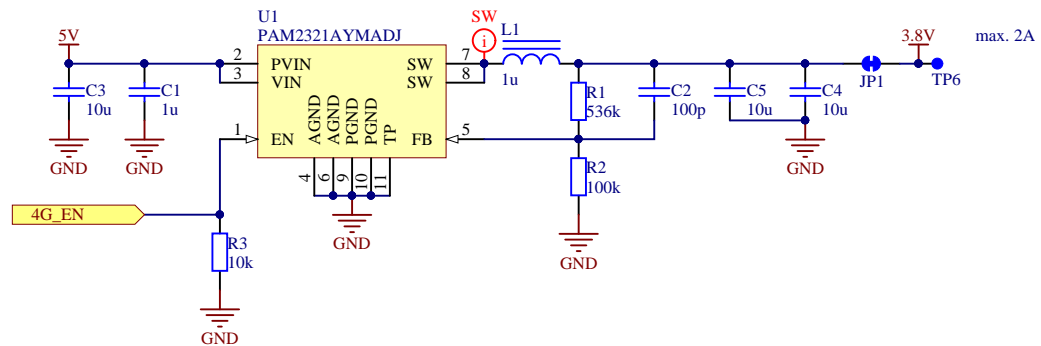
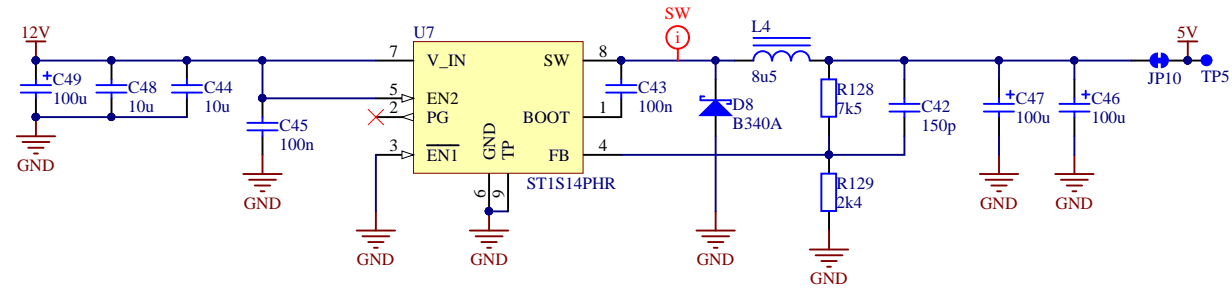
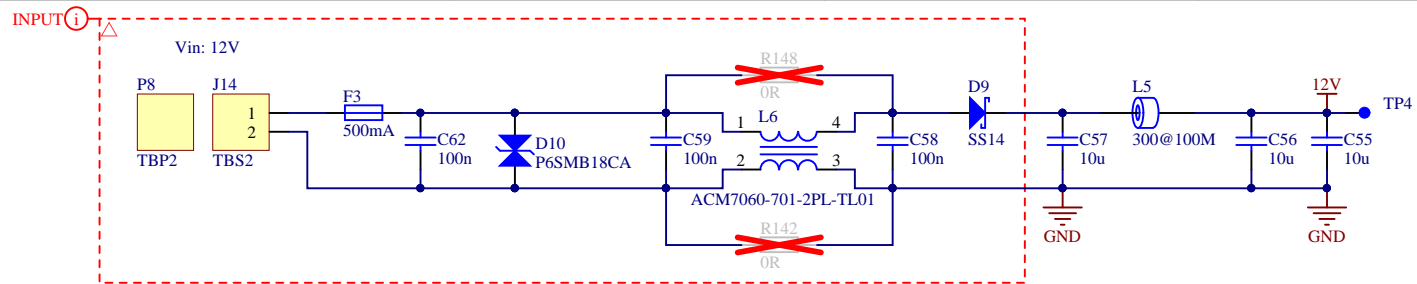


▲ przy montażu SIM rezystor z sim_cd dac na DNI



Title		Micro SD Card Socket	
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Title Power			
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